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Systems

SPECTRA 70

70/668 CCM AND 70/700 SERIES BUFFERS

Communication Controller-Multichannel (CCM) Communication Buffers Reference Manual

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1. 70/668-11, 21, 31 COMMUNICATION CONTROLLER-MULTICHANNEL (CCM)

GENERAL DESCRIPTION

◆ The Communication Controller-Multichannel (CCM) peripheral device multiplexes and controls the transmission of data to and from various remote terminals and systems. Figure 1-1 shows the physical location of the CCM with respect to the processor, communication line buffers, common carrier interface devices, and the remote I/O terminals.

The CCM is a multiplexing device capable of providing a distinct level of data and system control when used with the 70/35, 70/45, or 70/55 Processors. A single multiplexor trunk connects this device to its controlling processor. The CCM is capable of servicing a mixture of buffers with a total data rate transfer of 6,000 bytes per second.

A maximum of seven CCMs can be attached to the 70/35 Processor while the 70/45 and 70/55 Processors can accommodate up to eight CCMs. The actual number of CCMs used, however, is governed by the size of the processor memory, the number and data rates of the communication lines serviced by the CCMs, and the demands of other peripheral devices controlled by the processor.

There are three different models of CCMs. The CCM Model 70/668-11 has a maximum control capacity for 16 communication lines; the CCM Models 70/668-21 and 31 have a maximum control capacity of 32 and 48 lines respectively. The CCM services each communication line through a single buffer based upon the type of remote terminal or system with which it must operate. Two buffers are required for the termination of full duplex communication facilities. Each buffer is designated by a specific device address.

Utilizing the maximum number of CCMs per processor, a 70/35 Processor can simultaneously control and service 176 communication lines. Theoretically, the 70/45 and 70/55 Processors can control 240 communication lines. The actual limits of communication line servicing and control are dependent upon the types and data rates of the circuits involved as well as the memory size of the processor. A maximum of 16 different combinations of various remote terminals and communication line characteristics can be accommodated in a single CCM. In some instances the size of the individual buffers, and the particular combinations of these buffers, may cause physical limitations which result in systems where a CCM cannot physically service the number of buffers given as a theoretical maximum.

Although the maximum continuous CCM throughput is 6KB, the CCM can maintain a byte transfer rate to the processor of 50KB for a maximum of 60 consecutive byte transfers. This rate would be realized if all 20 lines covered by a single buffer scan cycle each produced a completely framed character for transfer to the processor and each of these characters required the generation of a two-byte coordination message.

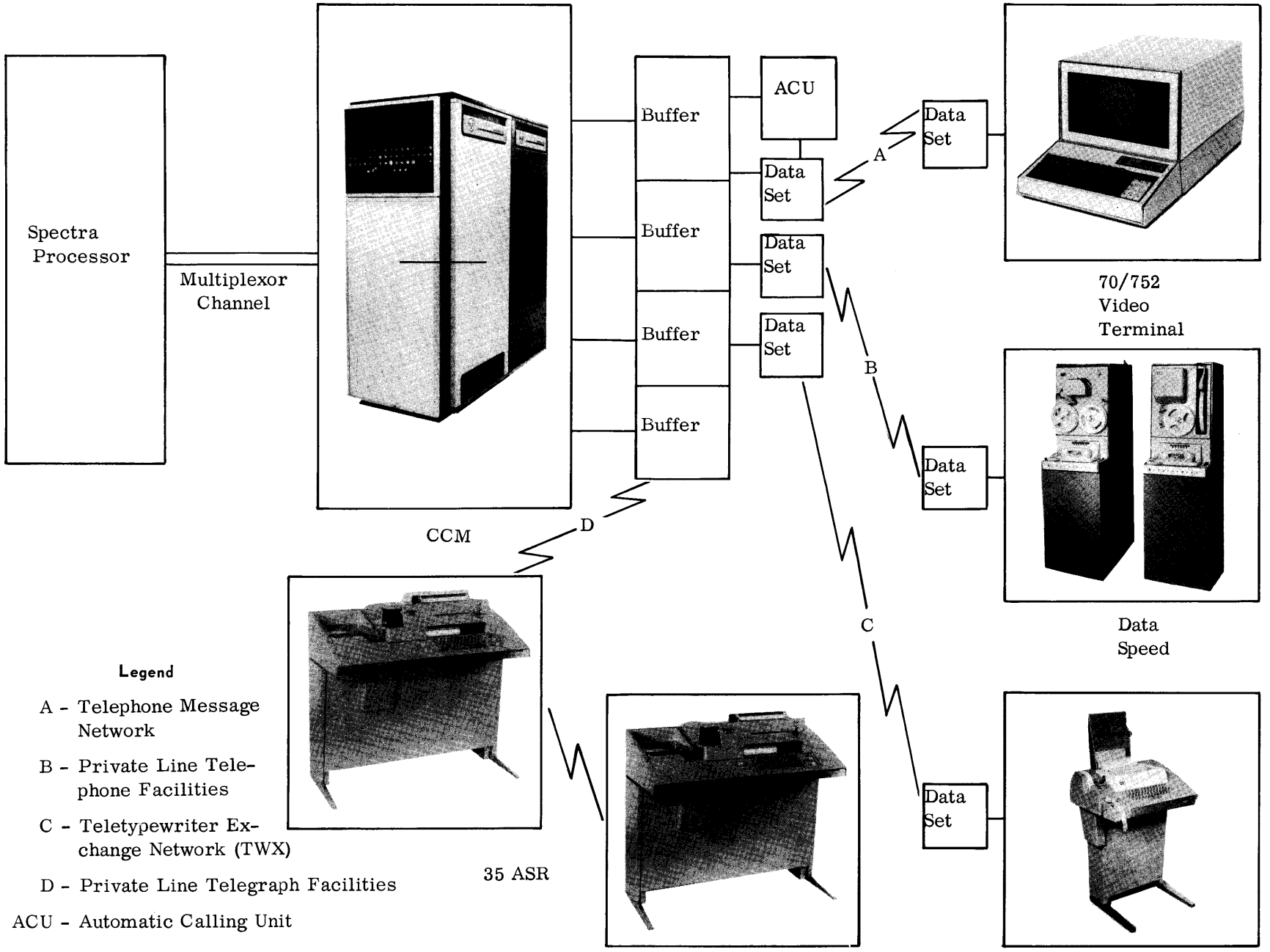


Figure 1-1. Spectra 70 Communication Layout

CONTROL ELECTRONICS

◆ The Control Electronics logic executes processor commands by exchanging the required signals with the buffers to effect a bit-serial data transfer across the CCM-Buffer interface. Character assembly and serializing are performed in the Control Electronics along with other logical operations required to execute the processor commands and generate the necessary terminations and interrupts to the processor.

A core memory within the CCM provides storage for data being transferred among the processor, buffers, and character accumulation/distribution areas, as well as counters and indicators. This memory has a read-regenerate, clear-write cycle time of 2 microseconds per word and contains 512 words, each word consisting of 18 bits including parity.

The Control Electronics supplies the pulses to the buffer which control the required bit timing or modulation rates for the communication lines. The modulation rates, which can be provided through oscillator sets for various applications, are as follows:

Oscillator		Modulation Rates
Set	Frequency	(bits per second)
1	76.8KC	2400, 1200, 600, 300, 150, 75
	64.0KC	2000, 250
2	57.6KC	1800
	33.6KC	1050
3	4.27KC	134.4
	5.82KC	45.5
4	3.64KC	56.9
	3.52KC	110
*5	57.6KC	1800
	30.72KC	960

*Set 5 is not supplied except when specifically required. Its use necessitates the removal of either set 2 or set 3.

Buffer Scan

◆ The total system capability provided by a Spectra 70 Communication System is a function of the variety of remote terminals employed, the types of communication lines which are utilized, and the transmission rates which must be maintained. The transfer of data and control signals to and from the buffers is accomplished by means of a CCM line scan. This function scans the first 16 buffers in any CCM at a higher priority rate than the remaining buffers attached to that CCM. All communication lines, buffers, and device addresses can be considered to be assigned within a high-speed group or a low-speed group. The first 16 lines are considered the high-speed group and lines 17 through 32 or 48 are considered the low-speed group. In the 70/668-11 all 16 lines are scanned at the high-speed rate, but this does not restrict low-speed circuits and

Buffer Scan *(Cont'd)*

terminals from use with this CCM. For the 70/668 Models 21 and 31, the line scan is always the first 16 lines followed by the next four lines of the low-speed group. This sequence is followed until all 32 or 48 lines have been serviced and then the cycle repeats itself.

Example: CCM Model 70/668-21 (32 lines)

Line Scanning Sequence:

1-16 and 17-20, 1-16 and 21-24, 1-16 and 25-28, 1-16 and 29-32, 1-16 and 17-20 etc.

Table 1-1 indicates throughput capacity for CCM Models 70/668-11, 21, and -31 based upon the required data rate of the communication lines used.

Table 1-1. CCM Throughput Capacities

CCM Model(s) 70/668-	Low-Speed Group (17-48)			High-Speed Group (1-16)			
	Highest Speed Line - bps	Lines Permitted	Turnaround Delay (ms)	Highest Speed Line - bps	Lines Permitted	Turnaround Delay (ms)	Total Lines Permitted
11	-	-	-	2400	16	3.4	16
21, 31	2400	4	4.2	2400	16	4.2	20*
21, 31	1800	4	4.2	2400	16	4.2	20*
21, 31	1200	8	8.4	2400	16	4.2	24*
21, 31	1050	8	8.4	2400	16	4.2	24*
21, 31	960	8	8.4	2400	16	4.2	24*
21, 31	600	16	17	2400	16	4.2	32
31	300	32	33	2400	16	4.2	48

*Requires wiring change. Can be accomplished in field.

Note:

The turnaround delay shown in table 1-1 represents the maximum delay caused by CCM hardware in issuing a new command to the buffer when command chaining is used.

As indicated in table 1-1, CCM Models 21 and 31 (32 and 48 lines) can control a maximum of 20 (and 24) communication lines if all 16 lines of the high-speed group are 2400 baud circuits and the 4 lines of the low-speed are either 2400 or 1800 baud circuits. This control capability is increased to 24 lines if the 4 low-speed lines are either 1200 or 1050 baud circuits. In these instances, the scan rate of these CCMs would be reset at 20 or 24 by a field or factory wiring change. This assures sufficient scan time to service these high-speed circuits by eliminating the scanning of the remainder of the higher order unused line positions on these CCMs.

CCM Device Addresses

◆ A list of suggested rules for implementing the assignment of device addresses for processor systems utilizing CCMs is as follows:

1. All device addresses used by CCMs must start in an upward sequence beginning at a number divisible by 16 (16 to 255). The first 16 device addresses on a system must not be assigned to communication lines but may be assigned to peripherals and CCM common device addresses. It should be remembered, however, that address $(00)_{16}$ should always be used for the console typewriter.

2. The identification for device address 255 is $(FF)_{16}$. Because this could create confusion with the error indication when coordination messages are generated for this device address, it is not advisable to assign it to an active line.

3. The CCM line (buffer) scan can be reset at any point. It is advisable to consider this in those cases where the number of lines serviced by a CCM is less than the total line servicing capacity of that device. By doing this the CCM eliminates the unused buffer scan positions from its scan cycle.

4. If multiple CCMs are attached to a system, peripheral device address assignments should not be made between the first device address of the first CCM and the last device address of the last CCM.

5. Device address assignments within a CCM servicing sequence should be contiguous. If not contiguous, a dummy line status word must be recorded in memory for each device address not used.

6. In systems involving multiple CCMs, the high-speed communication lines should be concentrated into one CCM, if possible, and this CCM should be assigned a higher priority multiplexor trunk so that it would be serviced before the other CCMs which control lower speed lines. Refer to the 70/35, 45, 55 Processor Reference Manual (No. 70-35-601) as to the servicing of multiplexer channels.

7. Common device address assignments for CCMs on multiple CCM systems need not be contiguous or restricted to any specific sequence. However, such assignments must be outside the range of device addresses assigned to communication buffers.

Coordination Message Line (CML)

◆ In order to provide for Processor-CCM coordination and initialization, a device address is used for control of each CCM. Assignment of this 'common' device address is independent of the buffer device address assignments and may be selected from any unused address outside the address range assigned to buffers. Command chaining is not permitted in connection with the CML.

OPERATIONAL CHARACTERISTICS

Line Status Words (LSWs)

◆ The CCM performs line control functions as directed by a wired-in program and line status words (LSW) stored in the CCM memory. These line status words, which are initialized by software, also provide the means for program designation of communication lines and remote terminal characteristics which must be administered by the CCM. Once initialized, LSW bits are set and reset by hardware action. The control responsibilities of LSWs are directly related to each communication line and its associated buffer. These designations are called systems classification. One set of six active and two spare LSWs is provided for each line, with each active LSW consisting of 18 bits including one parity bit. There are no LSWs associated with the common device address. The breakdown of the LSWs is detailed in Section 3, table 3-4.

Operational Words (OWs)

◆ An OW defines a specific operation or series of operations which the CCM is required to perform under a certain set of circumstances. OWs are referenced by the CCM program upon detection of the presence of a character or character sequence which requires special handling.

OWs are completely under the control of the basic software considerations that have been initialized for the communication requirements of systems and remotes controlled by any CCM. Unlike LSWs, OWs are not set and reset by CCM hardware. The necessary hardware functions are performed as a result of the initialized OW bit settings and not for the control of any particular communication line.

Each CCM can accommodate up to 64 two-word sets of OWs (OW-1 and OW-2) as necessary. Each OW contains 18 bits including parity. (See Section 3, tables 3-5 and 3-6.)

PROCESSOR - CCM CONTROL

◆ The processor initiates start device and halt device instructions along with a number of command codes to control the operation of the CCM and associated buffers.

Command Codes

◆ Processor command codes which require a response from the CCM are listed in table 1-2. The processor transfers these codes over the data out (DOUT) lines to the CCM, which then takes the necessary action.

Command Codes *(Cont'd)*

Table 1-2. Processor Command Codes

Bit Configuration								Command	Legal for
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0		
X	X	X	0	0	0	0	1	Sense	All Device Addresses
X	X	X	0	0	0	1	1	Write	All Device Addresses
X	X	X	0	0	1	0	1	Read Forward	All Device Addresses
X	X	X	0	0	1	1	1	Write Control	All except CML
X	X	X	X	0	1	1	0	Send Status	All Device Addresses
X	X	X	X	1	0	0	0	No Operation	All Device Addresses
1	0	0	0	0	0	0	0	Who Are You	All Device Addresses
0	0	1	0	0	0	0	0	Set Interrupt	All Device Addresses
X	X	X	0	0	0	1	0	Read Reverse	CML only

Note:

X in the above configurations can be either 1 or 0.

Sense Command

◆ This command initiates a transfer of the secondary indicator byte from the CCM to the processor on the "data in" (DIN) lines. Setting of the bit significance of the Sense command indicators to:

$2^7\ 2^6\ 2^5\ 2^4\ 2^3\ 2^2\ 2^1\ 2^0$

0 0 0 0 0 0 0 1

indicates an illegal operation which includes all command codes not defined in table 1-2 and all Write Control bytes not defined in table 1-3. Burst mode is an illegal operation for the CCM.

Write Command

◆ This command is decoded by the CCM to condition the buffer to transmit. The CCM then generates service requests as necessary to accomplish the transmission. The CCM memory is loaded by issuing a Write command to the common device address.

Read Forward Command

◆ When this command is issued for the common device address, the CCM is placed into the Normal mode and permits the processor to receive coordination messages (CMs) from the CCM. For all other device addresses this command causes the CCM to condition the buffer to receive, and upon demand from the CCM, to transfer received data to the CCM.

Write Control Command

◆ This command is used by the processor to perform certain control functions in the buffer. The CCM interprets the first data byte of this command as a command for the addressed buffer. Additional data bytes may follow the first, depending upon the function to be performed. The Write Control command is always terminated by the processor.

Table 1-3. Write Control Bytes

Function	Bit Configuration 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0	CCM Action	Additional Bytes
Auto-Call	0 0 0 0 0 0 0 1	Auto-Call (ACC) to buffer.	Dialing Information.
Suppress Start Stop	1 0 0 0 0 0 0 0	Transmit (TC) to buffer. Suppress start and stop bits, to permit timed spacing and/or marking intervals on the line.	As required for appropriate time generation.
Disconnect	0 0 1 0 0 0 0 0	Disconnect (DISC) to buffer to break existing connection on communications line.	None.
Acknowledge	0 0 0 0 1 0 0 0	Acknowledge (ACKC) to buffer. Buffer generates timed ACK signal.	None.

The number of bits of each additional byte transferred to the buffer is controlled by the bit configuration. All bits are transferred from 2^0 up to, but not including the highest order bit which is equal to 1.

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0	0	0	1	X	X	X	X
1	X	X	X	X	X	X	X

The bits transferred in each additional byte are represented in this example by X. These bits may be either 1 or 0.

The additional byte used for Auto-Call consists of only four bits which are the binary configuration of a number used in the dialing sequence. Numbers must be transferred between the buffer and the common carrier's dialing equipment in bit parallel due to the interface requirements of the automatic dialing equipment.

Write Control (Cont'd)

When performing suppress start/stop functions, the CCM must transfer the additional bytes to the buffer at the bit rate called for by the buffer. Any start or stop bits will be suppressed. In this manner, a variety of on-off sequences can be created for the communication line. The following is an example of how this method can be used to create sequences for an 80ms break, an 80ms pause, and a 160ms break for a 70/710 Telegraph Buffer operating with a 75 baud (100 wpm) telegraph line.

At 75 baud, the duration of each bit of the 5-level Baudot code is approximately 13.5ms. Therefore, 6-bit times are necessary to create a positive sequence of 80ms duration.

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	
1	1	0	0	0	0	0	0	(Byte 1)
1	0	0	1	1	1	1	1	(Byte 2)
1	0	0	0	0	0	0	0	(Byte 3)
0	0	0	0	1	0	0	0	(Byte 4)

All bits in the byte, up to, but not including the last bit in the byte, are sent to the buffer.

In this example, 2^7 is considered as the last bit in the byte. Parity is not included for determination of the time sequence. The 80ms break is created by the six 0's of byte 1, the 80ms pause by the 1 bit in the 2^6 position of byte 1, and the first five 1 bits of byte 2 (2^0 to 2^4). The 160ms break (12 bits in this case) is created starting from the 0 in bit position 2^5 of byte 2, running through all the bit positions of byte 3, (except 2^7) and the first three 0's of byte 4 (2^0 to 2^2).

The commands listed below are transmitted to the CCM via the multiplexor channel.

Send Status Command

◆ This processor command causes the standard device byte to be sent to the processor on the "Data In" (DIN) lines. Refer to Section 3, table 3-1 for standard device interpretation.

No-Operation Command

◆ This command from the processor causes the standard device byte to be sent by the CCM to the processor.

Who Are You? Command

◆ This command from the processor causes the CCM to place the address of the line for which the service request has been issued on the DIN lines, and resets the interrupt signal.

The processor always responds to PCI or normal interrupt with WRU. The device causing the interrupt responds with its device address. This, in turn, resets the interrupt in the processor and then the CCM responds with RDY.

Set Interrupt Command

◆ This command from the processor causes this unit to reset the END signal and to set the interrupt line.

Read Reverse Command

◆ This command from the processor initiates the transfer of the contents of CCM to the processor. This command is valid only for the CCM Common Device Number.

DATA TRANSFER

Character Assembly and Serialization

◆ All data transfer between the CCM and buffers, in either direction, is serial by bit. The assembly of incoming bits and serializing of outgoing characters are performed by the CCM. The first data bit received from the buffer occupies the low-order bit position of the byte being assembled. In cases where the remote terminal or the buffer alters the sense or sequence of the bits, the programmer must make appropriate conversion in the processor. Data is transferred over communication circuits in either asynchronous or synchronous operation.

Asynchronous Operation

◆ The information bits of each character are preceded by a start framing element and followed by a stop framing element of one or more units or bit times. These character framing elements are transferred between the buffer and the CCM, when receiving, but are deleted before the character is transferred to the processor by the CCM. When transmitting data to the communication line, the required framing bits are generated by the CCM. System classification bits, set by the program in the LSW for each line, identify the code structure used on that line. (See Section 3, table 3-3.)

Synchronous Operation

◆ No character framing elements are used in synchronous operation. Once synchronization has been established, each series of consecutive bits (number bits per character as defined by system classification) are handled as discrete characters without further framing considerations. Various rules for establishing and maintaining synchronization are invoked by the assigned system classification for the synchronous systems which can be handled by the CCM.

In some systems, synchronization is established entirely by the CCM without program involvement. When receiving bits from the buffer, the CCM assembles the number of bits specified by systems classification and tests for the wired-in idle line or synchronizing character (SYN). If SYN is not present, the new codes resulting from reassembly of a new character as each succeeding bit is received are tested, until SYN is recognized. The sequence counter is then incremented. If the next character is SYN, synchronization is presumed to be established. If a character other than SYN is received, the counter is reset to 0 and testing for SYN will proceed on a bit basis.

Synchronous Operation (Cont'd)

When transmitting synchronously, the CCM generates and transmits seven SYN characters preceding the data. Once synchronization is established, SYN is generated as necessary to maintain continous transmission at the synchronous rate.

A given system may require the generation of a number of SYN characters beyond the counting ability of the CCM. In this case the processor program must generate SYN. Synchronization is not presumed to be established, in this type of operation, upon recognition of a specific number of SYN characters, but only upon recognition of a discrete character which indicates the end of the SYN sequence. This recognition is reported to the program by the CCM for appropriate action. Incoming SYN characters are recognized by the CCM and deleted from the message.

When parallel buffers (bit-parallel data transfer to an from the communications line) are used, the CCM operates synchronously to the extent that no character framing elements are used. Special characteristics of the remote device or the facility obviate the use of SYN characters to establish or maintain synchronization. The result is that this line appears always in sync so that no SYN characters need be generated by the remote device and there is no SYN generation by the CCM.

Channel Coordination

◆ The maintenance of orderly data flow is accomplished by the CCM by use of the following tools:

1. System Classification established by software and stored in the Line Status Words. (See Section 3, table 3-3.)
2. Wired-in decoding logic which generates one of up to 64 discrete CCM memory addresses (OWs) for each combination of inputs. Each memory address permits access to expressions of further CCM action. Figure 1-2 identifies the inputs to this logic having particular significance to the programmer.

   During Read operations, the character to be decoded has been assembled by the bit accumulator/distributor and modified as per system classification as to shift status etc. The parity is maintained with the same sense as received over the line.

   During Write operations, the character at this point has the same bit configuration as when received from the processor except with USASCII, where the 2^8 bit will have been preset so that when the conversion to extended ASCII to USASCII is subsequently performed, the character will have correct line parity.

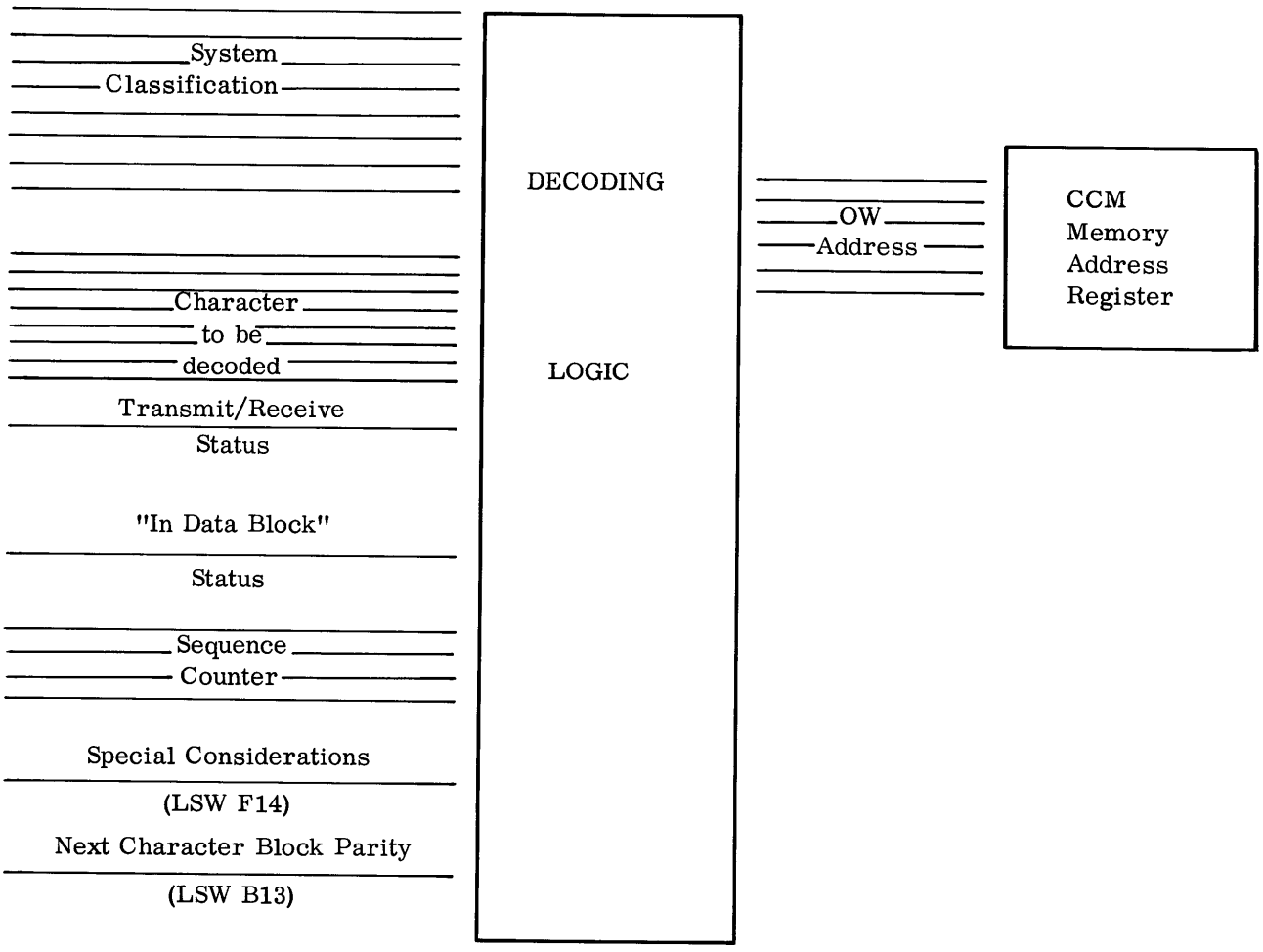


Figure 1-2. Generation of OW Address

Channel Coordination *(Cont'd)*

3. Operational Words (OW) established by the program and stored in CCM memory. The OWs direct further CCM action and are addressed as described in 2. above and in Figure 1-2. Up to 64 two-word sets (OW-1, OW-2) may be provided for each CCM, with each word comprising 18 bits including parity. The breakdown of the OWs is given in Section 3, tables 3-5 and 3-6.

4. The In Data Block (NDB) indicator bit in each set of LSWs permits two different OWs to be accessed upon recognition of a specific control character as a means of generating discrete actions. All characters which cause fetching of an OW are transferred to the processor regardless of the setting of NDB, unless inhibited by the OW. For systems which do not use the NDB control function, the bit must be set upon initialization of CCM memory by the program.

   In systems using the NDB control function, the bit is set and reset by OW. It will be reset, where called for by systems classification, by processor initiation of a Read, Write, or Write Control command but not as a result of command chaining.

5. Sequence Counter: Four different sequence counter indications permit the accessing of four different OWs for any given combination of system classification, character recognition, and transmit/receive status. This capability enhances recognition of multi-character sequence recognition.

6. Special Considerations (LSW F14): This consideration is applicable only to use with certain systems where specific control characters which must be recognized for functional purposes, can also be used as data characters in the text of the message. Refer to table 3-4.

7. Next Character Block Parity (LSW B13): This indication specifies that the character following it is to be recognized as a block parity character.

After each incoming character is transferred to the character transfer store area of the LSW B, and each outgoing character is received from the processor, it is decoded as described in 2 above. If a hit results, the addressed OW-1 is fetched and appropriate action is taken as indicated in table 3-5. If indicated by OW-1, OW-2 is also fetched to provide required additional information. If no hit results, the character has no channel coordination significance and is handled as data.

Certain operations called for by system classification are performed by the CCM without reference to OWs. The upshift and downshift functions of IBM 1050 and 2741 systems and the Figs and Ltrs functions of Baudot coded telegraph equipment are performed directly by CCM logic. These shift functions are inserted automatically when transmitting. If it is desired to exclude these shift characters from the processor when receiving, the proper OWs must be established. The detection and generation of SYN where appropriate in synchronous systems are performed by CCM logic without reference to OWs. Except for the exclusion of shift

Channel Coordination *(Cont'd)*

characters, the programmer's only responsibility in relation to these functions is to designate the proper system classification during initialization.

The selection of the characters to be decoded by the logic referred to in 2. above is made at a time specified by standard RCA EDP Procedures.

Service Requests

◆ The transfer of data to the processor accumulated as a result of the line (buffer) scan operation, and the acceptance from the processor of outgoing data, is accomplished by the CCM through the use of service requests to the multiplexor channel. Similarly, the reporting of coordination messages is also accomplished in this manner.

Processor Scan

◆ The processor scan cycle, meshed with the buffer scan to avoid contention with access to CCM memory, insures the orderly servicing of all lines. The reporting of coordination messages, if required, follows the completion of service requests, and precedes the advancing of the scanner.

The processor scan deals with whole characters, as opposed to the buffer scan which is concerned primarily with the assembly of the individual incoming bits when receiving and the serializing of the character by bit to the buffer when transmitting. The processor scan involves all LSWs of CCM memory except LSW A.

At fixed intervals the CCM checks the status of the standard interface to determine if any previous transfer has been completed. If data transfer is permitted, the LSWs of each successive line are scanned in a predetermined sequence until the next line that requires service by the Processor is encountered and the cycle repeated. Access to LSWs by a processor scan is arranged so that the buffer scan does not compete with the processor scan for access to CCM memory.

Character modifications, as specified by system classification, in handling parity bit and shift status bit are performed before requesting service from the processor.

When the received character is recognized as a control character, established for specific decoding, the CCM takes the necessary actions specified by the operational words. If the character is to be transferred to the processor, the procedure outlined above is followed.

If the character transfer has not been completed within a character time, the new character is discarded and an error is reported to the program as a coordination message.

Processor Scan
(Cont'd.)

Receive

◆ Data received from the line is transferred from the buffer serially by bit into an accumulator which then transfers the bits in parallel to the character assembly area of LSW A. The assembled character is then shifted to the Character Transfer Store area of LSW B to await transfer to the processor. Characters which are recognized by the decoding logic as data and control characters which are to be sent on into main memory, are transferred to the processor from this intermediate storage.

Transmit

◆ After the last bit of a data character is transmitted to the buffer, the character in the character transfer store is transferred to the bit accumulator distributor and during the next processor scan service for this line a service request is initiated when the character store is empty. When a service request is honored by the processor, the LSW of successive lines are examined and if a new character is required, the above will be repeated with the following exception:

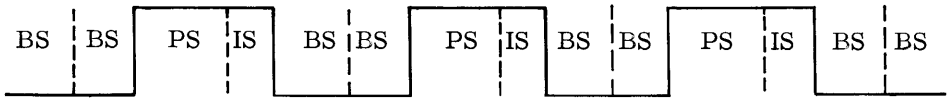
When the last character to be transferred is a control character which indicates that a block parity character is to follow, service request for that line is suppressed and the accumulated block parity character is transferred to character transfer store and subsequently to the communication line.

As determined by system classification, the 2^7 bit of the character transferred from the processor is compared with the shift bit in the LSW and a shift character, if required, precedes the character to be transmitted.

When a new character has not been obtained within a character time, in synchronous systems, an idle-line character is generated to replace the missing character; with asynchronous systems, a marking condition is maintained on the line.

Interrupt Scan

◆ The interrupt scan can be considered part of the processor scan, and like the processor scan, its functional position is between the CCM memory and the standard interface of the multiplexor channel of the processor. The interrupt scan follows a continuous cycle of the CCM memory addresses 1 through 48, whereas the processor and buffer scans follow the 1-16, 17-20, 1-16 pattern previously described under the buffer scan. There are actually two buffer scans for each processor/interrupt scan as shown in the following diagram.



where: BS = Buffer Scan
PS = Processor Scan
IS = Interrupt Scan

Asynchronous Transmission From Remote Device to Buffer

◆ When a Read command is issued to the buffer, it begins to examine the communication line for evidence of a mark-to-space transition indicating the presence of data on the circuit. Detection of a start bit by the buffer causes it to go RDY to the next Select. The CCM accesses the appropriate LSWs, determines input/output status, and places the received start bit in the character assembly area (LSW A). The buffer scan is then advanced to the next buffer.

In accordance with the bit timing, the buffer detects the first data bit of the incoming character, and responds with RDY to the next Select. The first data bit is transferred to the character assembly area. This routine of bit transfer is repeated until the complete character has been accumulated in LSW A (as specified by system classification). The contents of the character assembly area are examined to insure that the character is properly framed (presence of start and stop bits) which indicates a valid character.

The character is then transferred to the character transfer store (LSW B) and the character assembler is cleared to receive the next character. All of these events are accomplished by the buffer scan. All subsequent handling of this character by the CCM is accomplished during the processor scan intervals. The character transfer store area is examined by the processor scan and, if a character is present, character parity checking and block parity accumulation are performed during the processor scan.

The bit configuration of this incoming character is compared against previously wired-in decoding logic.

The decoding logic permits the accessing of operational words. If the character is recognized as not to be decoded, it is treated as data. If the character is recognized as a character which accesses as operational word, the appropriate action takes place as specified in that OW.

If the new character is a data character, or a control character to be transferred to the processor, it is stored in hardware registers associated with the standard interface; and the service request is set on the multiplexor channel.

If this is a data character not to be transferred to the processor, as a result of an Ignore specified by an OW, the character transfer store is cleared and no service request is sent to the standard interface.

The actual transfer of a character to the processor across the standard interface will be done in response to the appropriate signals from the multiplexor channel. The processor scan is not advanced until the service request is honored.

Asynchronous Data Transfer From Processor to Buffer

◆ When a Write command has been issued to the buffer, the processor transfers the first character over the multiplexor channel into a hardware register within the CCM. During the next processor scan the character is passed into the decoding logic which determines its identity as a data character or a character which must access an operational word.

Asynchronous Data Transfer from Processor to Buffer *(Cont'd)*

If it is recognized as a data character, it is placed in the character transfer store area of Line Status Word B. The buffer scan transfers the character in Line Status Word B to the character assembly area of Line Status Word A upon sensing that Line Status Word A is empty. Line Status Word B, including bit 14, is reset upon completion of this transfer. The contents of Line Status Word A will subsequently be passed to the buffer, one bit at a time, under control of the RDY signal from the buffer.

Data Accuracy Control

◆ Each incoming character is checked in the CCM for correct parity if specified by system classification. All correct parity characters or non-parity characters are modified, if necessary, to reflect odd parity before transfer to the processor. For each character failing the parity checks and $(FF)_{16}$ is substituted. Incoming character parity errors are reported to the program as a bad message by coordination message at the end of the block or message.

The CCM checks the parity of all characters transferred from the multiplexor on the DOUT lines. Data characters in error are transmitted to the remote device and a coordination message is generated. The error is reported in the communication reporting byte (CRB) as a bad message at the end of the block. This also applies to incoming characters from asynchronous operation.

Block parity, where used, is checked on incoming data and errors are reported when detected. With systems having both character parity and block parity, a single error indication is given to the program at block parity time when any combination of character parity or block parity errors have occurred. Block parity is generated for each outgoing block where such action is called for by the 2^2 bit of OW-2 as generated by the end of message character.

The transfer and checking of the block parity character are controlled by the operational words. The actual sensing of block parity status is controlled by the setting of LSW bit B13, as a result of end-of-message detection, which indicates that the character to follow is the block parity character. See Section 3, table 3-4.

In systems which do not have block parity it is necessary to set the correct bits in OW-1 to access a CRB specifying receipt of a good message, if this acknowledgement is required. Otherwise, only the presence of a bad message will be reported. With systems using the additional block parity detection, the reporting of both good and bad messages is automatic, and it is not necessary to set bits 9-12 of OW-1 to access a CRB to report the proper detection.

Code Modification

◆ All character codes are transferred to and from the processor in eight-bit bytes, plus correct parity. Codes consisting of less than nine bits will be modified as follows on receive and in a corresponding manner on transmit. (See Section 3, Code Modifications.)

Code Modification *(Cont'd)*

1. Eight-Bit Codes: Correct parity is generated in the 2^8 bit position.
2. USASCII: Conversion to and from Extended USASCII is performed and correct parity is generated in the 2^8 bit position for the processor, and in the 2^7 bit position for the line.
3. IBM 1050 and 2741 Codes: The 2^7 bit is set to reflect the shift status established by the last shift character (upshift = 1, downshift = 0). Correct parity is generated in the 2^8 bit position. The shift characters may be deleted through OW action when receiving. They are automatically inserted as required when transmitting.
4. Baudot Code: The 2^7 bit is set to reflect the shift status established by the last shift character (Figs = 1 Ltrs = 0). Correct parity is generated in the 2^8 bit position. The shift characters are deleted by OW action when receiving, but are inserted automatically as required when transmitting.

Data Timeout

◆ Where required by systems classification, the CCM detects and reports to the program by a coordination message, the failure to transfer data to or from the processor for the applicable line over an interval of 20 to 24 seconds. The timer is started by a Transmit, Receive, or Auto-call command. It is reset by data transfer and turned off by termination. The timer is allowed to run, and will expire after the 20-second time duration mentioned above; thereby, generating a coordination message to the processor. It must be noted that the timer will continue to advance during the receipt of shift characters or other characters discarded as a result of OW action.

Detection of Pause and Break

◆ On certain systems a pause or break is deliberately generated by a remote device for signalling purposes. Where specified by system classification a marking condition (Pause) for one character time causes a discrete character (110000000) to be generated and stored in the character transfer store area. This character may be decoded and used to address an OW which specifies action direction by the program. A similar operation is performed for a spacing condition (Break) for one character time except that the generated character is (100100000). Any action available in the OW may be utilized by the program to establish the duration of marking or spacing intervals to be acted on or reported.

The bit configurations above are used only within the CCM. Pause and Break characters are received from the communication line as all 1 bits and all 0 bits respectively. OW action is required for the detection of Pause and Break characters when receiving data from the line. The transmission of pause and break characters is a function of Suppress Start/Stop Write Control command. Pause and break characters will be passed to the processor if In Data Block is set and OW action does not specifically discard pause and break.

PROGRAM NOTIFICATION

Interrupts

◆ The CCM can operate the normal I/0 interrupt mechanism using both the PCI and termination interrupts. Each interrupt is stored in the CCM memory and serviced, in turn, under control of an interrupt scan. The request for service of an interrupt, made by setting the Interrupt Lead, is not related in time to the Set Interrupt command or Set Interrupt Lead received from the processor. If the Interrupt Lead is not set or if it is set for a device other than the one reporting SR-END, the Set Interrupt command is recorded in CCM memory and reported by the normal interrupt procedure at a later time. The standard device byte provided for each interrupt is detailed in table 3-1.

Coordination Messages (CM)

◆ The variety of remote devices, transmission characteristics, and line conditions that may be handled by a Spectra 70 Communications System, requires the CCM to supply more information to the program than can be efficiently communicated through the normal I/O interrupt routine. To meet this need a two-byte coordination message is generated for events or conditions which must be reported to the program. The two bytes are a communications reporting byte (CRB) followed by the device address byte of the buffer (line) involved.

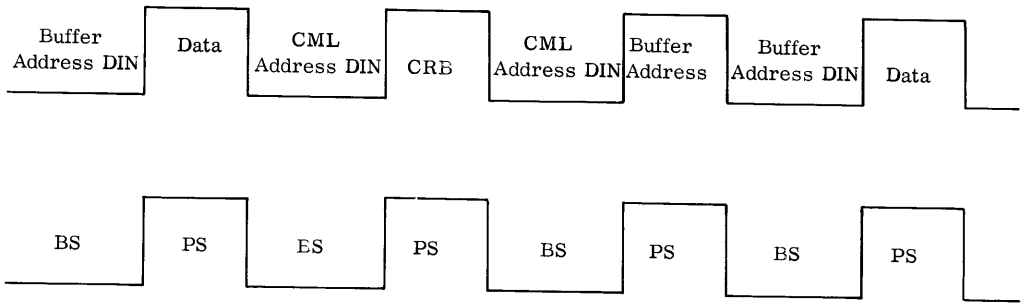
The coordination message line (CML) is assigned from any available device address, subject to restrictions, and is utilized for the coordination message (CM) reporting. After initialization the program must provide a Read command specifying the CML which was assigned to the CM before any commands are initiated for other device numbers. This Read command must be maintained continuously during the operation of the CCM. Interrupts requested for the CML are given priority in setting the interrupt lead but will not preempt an interrupt in progress. Upon completion of an interrupt service, the interrupt lead will be set for the CML immediately if a request had been received. In any case, the interrupt lead will not be set until after SR is set for the transfer of the second byte of the CM.

A breakdown of the CRB is shown in table 3-7. Except as indicated, bits 2^0 - 2^3 come primarily from the operational words, however, the good message/bad message indication can also be derived from the hardware logic with the good message indication being supplied in operational words, as in block parity systems. Bits 2^4 - 2^7 are set by logic to reflect detected conditions or status. CRBs are automatically generated as a result of a hardware error or malfunction, otherwise they must be specified by program if they are to be generated due to the recognition of certain conditions.

A delay is built into the CCM hardware so that the interrupt is not set until the service request for the second byte of the CM is set. Thus, the basic processor priority of service request over interrupt, assures that the entire CM (CRB + Device Address) is available to the program prior to interrupt.

The following diagram indicates the sequence in which the two-byte coordination message is passed to the processor as a result of handling incoming data, and the relationship of this operation to the buffer and processor scans.

Coordination Messages (CM) *(Cont'd)*



TERMINATION

CCM Initiated

- Termination is initiated by the CCM as a result of:

  1. An operational word.
  2. A buffer malfunction report.

As prescribed by the program in the LSW and OW, the CCM terminates commands as a result of its detection of appropriate conditions. In normal operations, when the prescribed conditions for termination are met, the CCM signals terminate (TERC) to the buffer on its next select.

The buffer responds with END after other conditions, if any, are met (see applicable buffer description). Following receipt of END from the buffer, the CCM signals END to the multiplexor in the normal manner. If Malfunction Report is reported by the buffer, the CCM signals END to the multiplexor immediately without further signal exchange with the buffer. If termination results from the receipt of a control character which is transferred to the processor and a CM is also required, the processor scan will be advanced following the transfer of the CM. END will be signalled when the processor scan subsequently returns to that line.

In special cases, when called for by system classification, termination of a Read command will be accomplished in the CCM without TERC being sent to the buffer. Receipt of a new Read command permits continuous buffer operation while accomplishing message segregation in the processor.

Processor Initiated

◆ When TERMINATE is received from the multiplexor, the CCM signals TERC to the buffer immediately if a Read command is being executed or if TERMINATE is accomplished by a NO-OP command (resulting from a Halt Device instruction). TERC is signalled upon transfer of the last bit when a Transmit or Write Control command with additional bytes is executed. The buffer responds with END after other conditions, if any, including timed delay, are met. (See applicable buffer description.) Following receipt of END from the buffer, the CCM signals END to the multiplexor in the normal manner.

Termination is initiated by the processor as a result of:

1. Byte Count = 0.
2. Halt I/O.

The sequence of termination for all of the above conditions, except malfunction and message separation is:

1. The CCM signals TERC to buffer.
2. The buffer signals END to CCM.
3. The CCM signals END to the computer.

For a malfunction condition, item 1 above is bypassed.

For a message separation condition, items 1 and 2 above are bypassed.

During normal operating conditions, termination results as follows:

1. When receiving data from the line:

   The CCM signals END to buffer immediately.

2. When transmitting data to the line:

   The CCM signals END to the buffer along with the last bit of the character in LSW A (character assembly area).

3. Termination with a Halt I/O condition:

   The CCM signals END to buffer immediately.

INITIALIZATION

◆ The CCM memory layout is in accordance with figure 3-1.

The entire CCM memory is initialized by program upon start of operations or on general reset following a PROP false indication on the standard I/O interface. If it is desired to make a program generated change to any LSW or OW, the entire memory is reinitialized.

A Write command is used by the program for initialization, employing the common device address selected for the handling of coordination messages. The initialization data sequence is as follows:

INITIALIZATION (Cont'd)

1. LSW spares (two words) initialized to all zeros.
2. LSW A for line number 1, followed by LSWs B, C, D, E, and F.
3. Repeat 1 and 2 above for all lines (2 through 48) regardless of the model CCM involved. All unused LSWs are initialized to all zeros, except bit 8 of LSW E which must be set to 1.
4. OW-1 and OW-2, sequentially as required. Each OW may be configured to produce the desired CCM action in accordance with the bit designations shown in table 3-5. Arrangement of OW's is established as provided for in RCA standard EDP Procedures.
5. The least significant six bits of the first two bytes and the least significant five bits of the third byte of a three byte sequence are used for each LSW. The CCM generates correct word parity in the 18 bit positions.

Byte	LSW Bits
1	0-5
2	6-11
3	12-16

Command chaining cannot be used in connection with the initialization Write command. Parity is checked on each byte transferred during initialization. A parity error causes termination of the Write command and the secondary indicator bit to be set in the standard device byte. Additional details concerning initialization procedures for LSWs and OWs are covered in Section 2.

When initializing the CCM, it is not recommended to operate another peripheral device on the multiplexor channel. This restriction does not apply to devices operating on selector channels.

CCM MEMORY READOUT

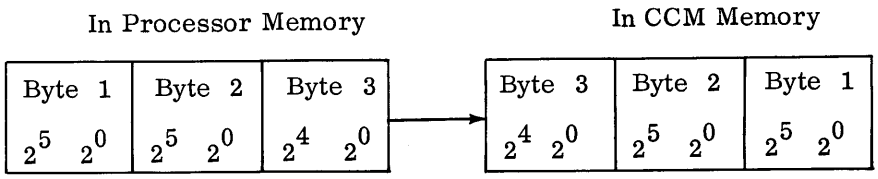
◆ The CCM responds to a Read Reverse command from the processor by reconstructing the bytes used for initialization, expanding as required with parity, and transferring them to the processor in the same sequence in which they were loaded. This operation results in a byte sequence in the processor reversed from the sequence which existed prior to loading.

2. CCM INITIALIZATION CONSIDERATIONS

CCM MEMORY

◆ The CCM control memory contains 512 words. This 512-word memory is divided into 48 sets of line status words and 64 operational word pairs. (See Section 3.) The line status sets are composed of six line status words, A through F, while operational words are two-word sets. Each word in both of these classifications contains 18 bits including parity.

When the LSWs (line status words) and OWs (operational words) have been established for any CCM, they are placed in processor memory and transferred to the CCM as shown in the following diagram:



LSWs must be transferred to the CCM memory in the particular sequence of their device addresses. OWs will be placed into the specific memory positions determined by the CCM installation specialists. These locations are determined after reviewing the OW requirements as specified by the programmer for each individual CCM. Standard RCA EDP Procedures contain the necessary instructions and other pertinent data for determining and documenting these requirements.

INITIALIZATION OF THE LINE STATUS WORDS

◆ Six line status words must be initialized for each active line on the CCM. However, since parity (17th bit) is generated by hardware, the programmer need concern himself only with initializing bits 0 through 16. Each LSW is loaded, a byte at a time, as shown below. The least significant bit in processor memory is the least significant bit position in CCM memory.

First Byte in bit positions 0 through 5

Second Byte in bit positions 6 through 11

Third Byte in bit positions 12 through 16

For control of remote communication systems, the LSWs are initialized by the user as follows:

All LSWs are set to 0 except:

Bit	Function
A15	Buffer Neutral Status
C0 thru C7	System Classification
C13	In Data Block

INITIALIZATION OF THE LINE STATUS WORDS (Cont'd)

For unused device addresses, the LSW specified below is set to 1.

Bit	Function
E8	Inactive Line

The C13 bit is set to 1 if the associated communication line is uncontrolled (where the remote terminal may initiate input at any time). C13 is set to 0 for communication lines which are controlled (where the processor has the control capability as to when input from the remote is initiated through polling, etc).

Figure 2-1 illustrates the loading of a complete set of line status words sequentially by bit, byte, and LSW. The two unused (spares) areas of CCM memory are loaded first followed by the six active LSWs in alphabetical order.

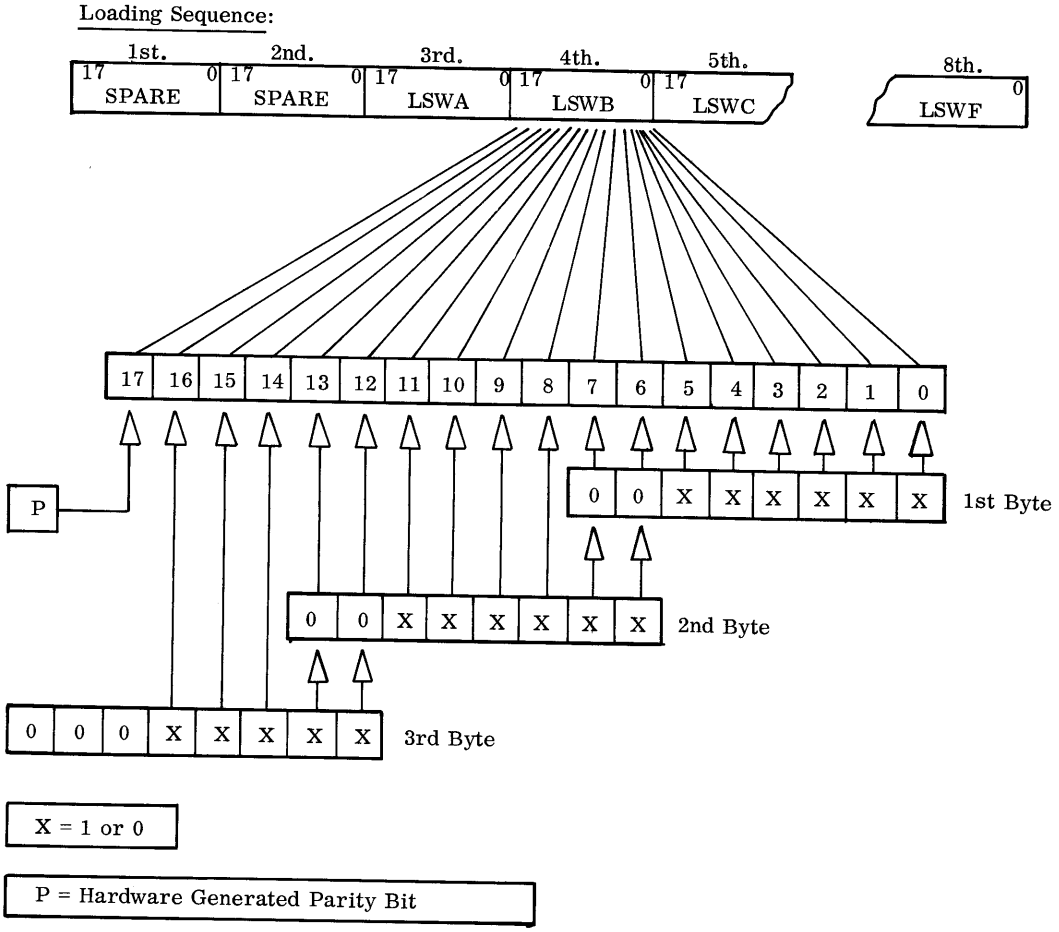


Figure 2—1. Loading of Line Status Words

CONSTRUCTION OF OPERATIONAL WORDS

General

◆ Operational words are referenced by the CCM program primarily for the determination of the presence of a specific character or character sequence which requires special handling. OWs are accessed only upon the recognition of a certain character that has been placed in the character transfer store (LSW B).

An OW defines a specific operation or series of operations which the CCM is required to perform under a certain set of circumstances. Both the operation and the condition under which they are to be performed are established by the programmer during CCM initialization. It is imperative, therefore, that the programmer fully understand the functions and operation of the remote device or system to be controlled.

Parity is checked after a character has been placed in LSW B and before the character is presented to the decoding matrix. Therefore, a bad parity character would not be recognized by this decoding logic and would not be detected as a character requiring an OW on those systems using parity. The bad parity character, in this case, would appear to be just another data character to the decoding logic.

Figures and Letters as OWs

◆ The appearance of Figures and Letters characters in the processor memory is controlled by the CCM in accordance with the requirements of any particular system.

1. If it is desired to discard these characters so that they do not appear in processor memory, they must be designated for decoding and the resulting OW-1 must indicate Ignore (bit 15 of OW-1 set to 1).
2. If it is desired to allow these characters to enter processor memory, no decoding and OW access is specified.
3. If it is desired that the program be advised upon the recognition of a consecutive number or sequence of a particular character, designated for decoding then these incoming characters must be accessed. A maximum of four consecutive identical characters can be utilized in this case for the accessing of an OW for such control purposes.

Delete Characters as OWs

◆ It is common for remote terminals which use USASCII to utilize the Delete Character as a fill character similar to the use of Letters by remote terminals operating with a 5-level Baudot code. USASCII Delete recognition can be used to access an OW and be discarded when received from the communication line. If CCM program recognition is arranged in this manner, it will prevent these Delete characters from reaching processor memory.

Operational Word Memory Address Assignments

◆ In advance of system delivery, a list must be developed of the control character bit configurations to be recognized and the corresponding input/output, in data block (NDB), and Sequence Counter (LSW F15, F16) settings which will result in the accessing of respective OWs. This information is used to provide the instructions for the necessary factory hardware wiring and advice as to the correct CCM memory address locations for OW initialization. (Refer to standard RCA EDP Procedures.)

OW CONSTRUCTION EXAMPLE NUMBER 1 (83-B-X)

◆ Table 2-1 is an OW table established for the proper CCM detection and control of a fictitious 5-level, semi-automatic, multistation, half-duplex, private line, telegraph system identified as 83-B-X. The control codes and control sequences which must be set into OWs have been defined as follows:

Function	Code
Start of Message (SOM)	ZCZC
End of Message (EOM)	NNNN
Start Code Answer-Back	V
End-of-Transmission Code (EOT)	S

The SOM and EOM perform their normal function, but because this system allows multiple messages in each transmission, the EOM of the last message is followed by an S. The V is received by the CCM from a remote terminal if that terminal has been polled, but has no traffic to send.

This particular example does not require the accessing of OW-2. The bit settings 0 through 16 of OW-1 are set to 1 or 0 to reflect the necessity of:

1 - take action

0 - do not take action

Based upon these OW requirements, the CCM hardware is set to reflect in the LSWs the bit settings for the initial conditions: Receive/Transmit status, NDB/out of data block, and the sequence counter.

OW-1 Explanation

V - Polling Answer-Back from Remote Terminal (No Traffic)

◆ 1. Receive/Transmit set to 1 - present only when receiving NDB to 0 - system should be out of data block when V is received. Sequence counter setting is not necessary when this character could be received.

2. OW-1 Bit Settings:

2, 1, 0 (Action Control) - 001, unconditional action.

3 - 0 Not Used.

4 - 0 V should not set NDB.

5 - 0 V should not reset NDB.

6 - 0 Do not inhibit resetting of sequence counter.

8, 7, - 00 will not effect sequence counter when bit 6 is set to 0.

Table 2-1. OW-1 Construction Example Number 1 (83-B-X)

Receive	Transmit	1	1	1	1	1	1	1
In Data Block	Out of Data Block	0	0	0	0	0	1	0
Sequence Counter (LSW 15, 16)		-	00	01	10	11	-	-
OW Bits		**Setting for V**	**Setting for Z (1st)**	**Setting for C (1st)**	**Setting for Z (2nd)**	**Setting for C (2nd)**	**Setting for N**	**Setting for S**
2, 1, 0 (Action Control)		001	001	001	001	001	101	001
3		0	0	0	0	0	0	0
4		0	0	0	0	1	0	0
5		0	0	0	0	0	1	0
6		0	0	0	0	0	1	0
8,7		00	11	11	11	00	11	00
12-9		0011	0000	0000	0000	0100	0101	0110
13		1	0	0	0	0	0	1
14		0	0	0	0	0	0	0
15		1	1	1	1	1	1	1
16		0	0	0	0	0	0	0
17 (Parity)		-	-	-	-	-	-	-

Note: Seven individual OW-1s must be constructed for control of this sytem.

OW-1 Explanation *(Cont'd)*

12-9 - 001 identical to $2^3 - 2^0$ of CRB (variable by program). Generate CM indicating receipt of V; therefore, V does not have to be stored in processor memory.

13-1 - Terminate existing command (Receive) because V means the connected remote terminal has nothing to send.

14 - 0 Exclude from BP count.

15 - 1 Ignore V so it will not be passed into memory.

16 - 0 OW-2 not required.

17 - Parity.

Z (1st) - First Character of Start of Message Sequence

◆ 1. Receive/Transmit set to 1 - present only when receiving NDB set to 0 - system should be out of data block when Z is received. Sequence counter set to 00 - Not incremented as of yet.

2. OW-1 Bit Settings:

2, 1, 0 (Action Control) - 001, unconditional action.

3 - 0 Not Used.

4 - 0 Z should not reset NDB.

5 - 0 Z should not reset NDB.

6 - 0 Do not inhibit resetting of Sequence counter.

8, 7 - 11 Trigger sequence counter upon recognition of this character.

12-9 - 0000 No action by CRB.

13 - 0 Do not terminate existing command (receive).

14 - 0 Exclude this character from BP count.

15 - 1 Ignore 2 so that it will not be passed to memory.

16 - 0 OW-2 not required.

17 - Parity.

C (1st) - Second Character of Start of Message Sequence

◆ 1. Receive/Transmit set to 1 - present only when receiving NDB set to 0 - system should be out of data block when C is received. Sequence counter set to 01 prior to the time C is received.

2. OW-1 Bit Settings:

2, 1, 0 (Action Control) - 001, unconditional action.

3 - 0 Not Used.

C (1st) - Second Character of Start of Message Sequence (Cont'd.)

4 - 0 C should not set NDB.

5 - 0 C should not reset NDB.

6 - 0 Do not inhibit resetting of sequence counter.

8,7 - 11 trigger sequence counter.

12-9 - 0000 No action by CRB.

13 - 0 Do not terminate existing command (Receive).

14 - 0 Exclude this character from BP count.

15 - 1 Ignore C so that it will not be passed to memory.

16 - 0 OW-2 not required.

17 - Parity.

Z (2nd) - Third Character of Start of Message Sequence

◆ 1. Receive/Transmit set to 1 - present only when receiving NDB set to 0 - system should be out of data block when Z is received. Sequence counter set to 10.

2. OW-1 Bit Settings:

2, 1, 0 (Action control) - 001, unconditional action.

3 - 0 Not Used.

4 - 0 Z should not set NDB.

5 - 0 Z should not reset NDB.

6 - 0 Do not inhibit resetting of sequence counter.

8, 7 - 11 Trigger sequence counter.

12-9 - 0000 No action by CRB.

13 - 0 Do not terminate existing command (Receive).

14 - 0 Exclude this character from BP count.

15 - 1 Ignore Z so that it will not be passed to memory.

16 - 0 OW-2 not required.

17 - Parity.

C (2nd) - Fourth Character of Start of Message Sequence

◆ 1. Receive/Transmit set to 1 - present only when receiving NDB set to 0 - system should be out of data block when Z is received. Sequence counter set to 11 prior to the time Z is received.

2. OW-1 Bit Settings:

2, 1, 0 (Action Control) 001, unconditional action.

3 - 0 Not used.

C (2nd) - Fourth Character of Start of Message Sequence (Cont'd)

4 - 0 Set NDB for all subsequent characters.

5 - 0 C should not reset NDB.

6 - 0 Do not inhibit resetting of sequence counter.

8, 7 - 00 Reset sequence counter (character sequence complete).

12-9 - 0100 Identical to 2^3 - 2^0 of CRB (variable by program). Generate CM indicating receipt of valid start of message sequence which would not have to be stored in processor memory.

13 - 0 Do not terminate the existing command (Receive) since data is expected to follow.

14 - 0 Exclude from BP count.

15 - 1 Ignore C so it will not be passed into memory.

16 - 0 OW-2 not required.

17 - Parity.

N - First Character of End-of-Message Sequence

◆ 1. Receive/Transmit set to 1 - present only when receiving NDB set to 1 - system should be set out of data block after N, which suffices for entire NNNN sequence, has been received since this is the end-of-message sequence.

Sequence counter setting is not necessary when this character could be received. Bits 6, 7, and 8 control the increment of sequence counter.

2. OW-1 Bit Settings:

2, 1, 0 (Action Control) - 101, action taken due to recognition that these successive N characters result in a valid four-character control sequence.

3 - 0 Not Used.

4 - 0 N's should not set NDB.

5 - 1 N's should reset NDB as end-of-message sequence under action control bits.

6 - 1 Inhibit reset of sequence counter so that all N's will be accumulated until the four-character sequence is recognized.

8, 7 - 11 Trigger sequence counter upon recognition of four successive N's.

N - First Character of End-of-Message Sequence (Cont'd.)

12-9 - 0101 Identical to 2^3 - 2^0 of CRB (Variable by program). Generate CM indicating receipt of valid end-of-message sequence which would not have to be stored in processor memory.

13 - 0 Do not terminate existing command (Receive).

14 - 0 Exclude this character from BP count.

15 - 1 Ignore N's so that they will not be passed to memory.

16 - 0 OW-2 not required.

17 - Parity.

S - End of Transmission Code

◆ 1. Receive/Transmit set to 1 - present only when receiving NDB set to 0 - system should be out of data block when S is received.

Sequence counter setting is not necessary when this character could be received.

2. OW-1 Bit Settings:

2, 1, 0 (Action Control) - 001, unconditional action.

3 - 0 Not Used.

4 - 0 S should not set NDB.

5 - 0 S should not reset NDB.

6 - 0 Do not inhibit resetting of sequence counter.

8, 7 - 00 Reset sequence counter (transmission is complete from this particular terminal).

12-9 - 0110 Identical to 2^3 - 2^0 of CRB (variable by program). Generate CM indicating receipt of valid end-of-transmission character. Therefore, the EOT character would not have to be stored in processor memory.

13 - 1 Terminate the existing command (Receive). The next command would be Transmit (Write) in order to poll next terminal in polling sequence.

14 - 0 Exclude from BP count.

15 - 1 Ignore S so it will not be passed into memory.

16 - 0 OW-2 not required.

17 - Parity.

OW CONSTRUCTION EXAMPLE NUMBER 2 (70/799 VIDEO TERMINAL)

◆ The following is an OW table established for the proper CCM detection and control of a fictitious remote video display terminal. In this example, the terminal can be one of a number on a multistation, half-duplex, private line equipped for polling operation from the processor. The control codes which must be set into OWs are defined as follows:

From Video Terminal to Processor	
Start of Message	STX
End of Message	ETX
Transmit Start Code Answer Back	EOT

This example, as described, requires the accessing of OW-2 on one occasion. The bit settings of the OWs are set to 1 or 0 to reflect the necessity of:

1 - take action.

0 - do not take action.

Based upon these OW requirements, the CCM hardware is set to reflect in the LSWs the bit settings for the initial conditions: Receive/Transmit, in data block/out of data block and the sequence counter.

From Video Terminal to Processor

STX - Start Message

◆ 1. Receive/Transmit set to 1 - processor receiving NDB set to 0 - system should be out-of-data block when STX is received. Sequence counter setting is not necessary when this character is received.

2. OW-1 Bit Setting

2, 1, 0 (Action control) - 001, unconditional action.

3 - 0 Not used.

4 - 1 STX should set NDB.

5 - 0 STX should not reset NDB.

6 - 0 Do not inhibit setting of sequence counter.

8,7 - 00 will not affect sequence counter when Bit 6 is set to 0.

12-9 - 0000 no requirement to advise processor of receipt of STX.

13 - 0 do not terminate existing command (Read).

14 - 0 Exclude this character from BP count.

15 - 0 Do not ignore this character.

16 - 0 OW-2 not required.

17 - Parity.

Table 2-2. OW-1 and 2 Construction Example Number 2
70/799 Video Terminal

1	0	FROM VT TO PROCESSOR		
Receive	Transmit	1	1	1
In Data Block	Out of Data Block	0	1	0
Sequence Counter (LSW F15, 16)		X	X	X

OW-1 Bits	Setting for STX	Setting for ETX	Setting for EOT
2, 1, 0 (Action Control)	001	001	001
3	0	0	0
4	1	0	0
5	0	1	0
6	0	0	0
8, 7	00	00	00
12-9	0011	0100	0101
13	0	1	1
14	0	0	0
15	0	0	1
16	0	0	1
17 (Parity)	-	-	-

Note:

Five individual OW-1's must be constructed for control of this system.

ETX - End Message

◆ 1. Receive/Transmit set to 1 - processor receiving in data block/out-of-data block set to 1 - system should be in NDB when ETX is received. Sequence counter setting is not necessary when this character is received.

2. OW-1 Bit Settings:

2, 1, 0 (Action control) - 001, unconditional action.

ETX - End Message (Cont'd.)

3 - Not used.

4 - 0 ETX should not set NDB.

5 - 1 ETX should reset NDB.

6 - 0 Do not inhibit setting of sequence counter.

8,7 - 00 Will not affect sequence counter when Bit 6 is set to 0.

12-9 - 0001 Identical to 2^3 - 2^0 of CRB (variable by program). Generate CM using these bit settings for CRB which indicate a good message indication upon receipt of ETX. This must be specified since this system uses character parity (CP) only.

13 - 1 Terminate existing command (Read) upon recognition of ETX from remote video terminal.

14 - 0 Exclude ETX from BP count.

15 - 0 Do not ignore this character.

16 - 0 OW-2 not required.

17 - Parity.

EOT - Start Code Answer-Back

◆ 1. Receive/Transmit set to 1 - processor receiving NDB set to 0 - system should be out-of-data block when EOT is received (placed out of data block by previous ETX). Sequence counter not necessary when this character is received.

2. OW-1 and 2 Bit Settings:

2, 1, 0 (Action Control) - 001, unconditional action.

3 - 0 Not Used.

4 - 0 EOT should not set NDB.

5 - 0 EOT should not reset NDB.

6 - 0 Do not inhibit setting of sequence counter.

8, 7 - 00 Will not affect sequence counter when bit 6 is set to 0.

12-9 - 0101 Identical to 2^3 - 2^0 of CRB (variable by program) - any configuration will suffice in this case. Generate CM indicating receipt of EOT.

13 - 1 Terminate existing command (Read) upon recognition of EOT from remote video terminal. Processor/CCM/Buffer would have been previously placed

EOT - Start Code Answer-Back (Cont'd.)

in the Write Mode after receipt of EOT in order to transmit the polling code; then to the present Read Mode in order to receive EOT.

14 - 0 Exclude this character from BP count.

15 - 1 Ignore this character (CM should suffice as evidence of receipt of EOT).

16 - 1 OW-2 is required.

17 - Parity.

3. OW-2 Bit Settings

Set Bit 3 of OW-2 to 1 - Set status modifier bit in standard device byte.

All other bits of OW-2 should be set to 0 in this case.

Use of the status modifier bit in conjunction with command chaining would be triggered upon recognition of EOT. Thus, the one-character Read would bypass the next command (multi-character read in anticipation of incoming data) and go to a one-character Write to send out the next polling code in the established sequence.

4. Other Considerations

In the general use of this application it is considered an advantage to allow STX and ETX to enter memory, as any normal data character without generating a CM. This may assist in keeping track of individual messages internally.

If it is desired to recognize STX as an error in the text of a message, an OW should be established specifically for STX in data block and to generate a CM.

If it is desired to eliminate STX under these circumstances, set Bit 15 of OW-1 to 1, unless it is desired to have it recorded for error analysis.

A decision must be made as to the handling in data block and STX-ETX. Arranging the OWs to set NDB on STX and out-of-data block on ETX would eliminate superfluous characters from coming into the processor; but if STX were to be lost coming in, no subsequent data would be recognized.

EOT - Start Code Answer-Back (Cont'd)

It is not necessary to inform the program through CMs of the presence of STX and ETX when transmitting data to a remote terminal. Since length of message is known, byte count will lapse upon EOM; (ETX) this automatically generates a CM. It would not then be necessary to check in data block because NDB is always valid during CCM transmit.

For systems employing merely a character parity check, only the bad message CRB (parity error) is generated automatically as a result of OW-1, bits 12-9. Therefore, the good message CRB must be specified by an OW generated CM if desired. Any appropriate EOM indication can cause access to an OW-1 specifying in bits 12-9, good message reporting. The CCM will then check for the setting of the error bit, and in its absence, will report a good message. In systems utilizing block parity both indications are automatic and the generation of a CM as a result of OW recognition is unnecessary. (See Data Accuracy Control, Section 1.)

RULES FOR PAUSE AND BREAK RECOGNITION

◆ Pause and Break duration detection, where required by the particular system involved, is implemented through the use of operational words.

Pause

◆ The three conditions under which Pause detection is normally required are:

1. When input from the remote device is generated as a result of manual keyboard operation: interrupted transmission is inherent. Therefore, the processor does not want to be notified on these frequent data lapses, nor does it want these Pause characters to enter memory.

   In this case the operational word specifies the deletion of all incoming Pause characters.

2. When input from the remote device is generated by an automatic tape transmitter: torn tape conditions can occur. In this case the processor should be notified immediately through the generation of a coordination message.

   The operational word may be set to recognize a specified number of sequential Pause characters, up to four. The resulting coordination message causes termination of the Read command to that buffer.

3. When a Pause of a certain duration is used for specific signalling purposes, a coordination message is generated as a result of operational word recognition.

   The operational word is set to recognize the specific number of Pause characters which create the particular signal.

Break

- Break detection is normally required under the following conditions:

  1. The generation of the break character as a result of an abnormal circuit condition or failure, commonly called an open line. Therefore, the processor should be notified immediately.

     The operational word may be set to recognize a specified number of sequential break characters, up to four if desired. The resulting coordination message causes termination of the Read command to that buffer.

  2. When the Break of a certain duration is used for specific signalling purposes, a coordination message is generated as a result of operational word recognition.

     The operational word is set to recognize the specific number of Break characters which create the particular signal.

3. REFERENCE INFORMATION

STANDARD DEVICE BYTE

Table 3-1. Standard Device Byte

Item	Bit	Meaning
Status Modifier	2^0	Enabled by operation word entered in SDB and sent to multiplexor upon receipt of any command. Reset when reported.
Device Inoperable	2^1	Set by $\overline{BOP}$ after initiation. Reset by Send Status. $\overline{BOP}$ causes termination of any existing command. ($\overline{BOP}$ is designation for buffer not operable.)
Secondary Indicator	2^2	Set when an illegal operation is detected. Reset by Sense command.
Device End	2^3	Set for all conditions (always 1).
Control Busy	2^4	Equal to device busy (2^5) except when CCM is busy with a previous instruction, then $2^4 = 0$, $2^5 = 1$.
Device Busy	2^5	Set by a command. Reset by set interrupt code.
Termination Interrupt Pending	2^6	Set by set interrupt code. Reset by send status.
Manual Request	2^7	Reset for all conditions (always 0) - Manual requests processed in coordination message.

CONDITIONS REQUIRING ACCESS OF STANDARD DEVICE BYTE

Table 3-2. Conditions Requiring Access of Standard Device Byte

Conditions	Standard Device Byte								I/O Instruction CC Results			
									Start Device			
	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Sense	Other	Test Device	Halt Device
Available	0	0	0	0	1	X	0	X	0	0	0	0
Inoperable Buffer	0	0	0	0	1	X	0	X	0	0*	0	0
Inoperable CCM**	---No Ready Signal---								3	3	3	3
Buffer Working	0	0	1	1	1	X	X	X	2	2	2	2
Termination Interrupt Pending	0	1	X	X	1	X	X	X	2	2	2	0
CCM Busy with Previous Instruction***	0	0	1	0	1	X	X	X	1	1	1	1

Notes:

*Instruction terminates after acceptance with inoperability noted by $2^1 = 1$.

**Absence of a Read command to common device address inhibits Ready signal on all other device addresses.

***The processor may issue commands to buffers at any time. The CCM accepts these commands and holds the information in hardware registers (single command storage for each buffer) until the processor scan reaches the address of the initiated device. Any attempt to issue a new command before the previous command has been removed from CCM memory by the buffer scan results in a reply from the CCM to the multiplexor of control busy which sets condition code 1 for the instruction.

The delay in handling an initiation varies with scan position up to the maximum of one character time. Thus, a high-speed line could be delayed up to 3.3ms while a low-speed line could be delayed up to 26.6ms.

SEQUENTIAL MODIFICATION OF USASCII TO EXTENDED USASCII

◆ 1. The USASCII character is received from the communication line and will normally be configured as a 7-level code plus a parity bit in the 8th level. See Example (1) below.

SEQUENTIAL MODIFICATION OF USASCII TO EXTENDED USASCII (Cont'd)

2. Under control of systems classification, the CCM extends this line code by deleting the parity bit (2^7) and expanding the character by shifting the 2^5 and 2^6 positions so that they become the 2^5 and 2^7 positions respectively. See Example (2) below.

3. The original 2^6 bit is then duplicated in the newly created 2^5 position making the character an eight-bit code. See Example (3) below.

4. The CCM then adds the correct parity in the 9th level (2^8) before the character is passed to the standard interface of the multiplexor channel. See Example (4) below.

(Example is the Letter D)

(1)

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
P	1	0	0	0	1	0	0

(2)

2^6	2^5	X	2^4	2^3	2^2	2^1	2^0
1	0		0	0	1	0	0

(3)

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	0	1	0	0	1	0	0

(4)

2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
P	1	0	1	0	0	1	0	0

SEQUENTIAL MODIFICATION OF IBM 1050 CODE

◆ The IBM 1050 code received from the communication line will be configured as a 7-level code with parity in the 2^6 bit (check bit). This parity bit is shifted by the transmitting terminal so it is the first bit received from the line. The 2^7 bit is added by the CCM to reflect the shift status established by the previous shift character. Upshift for 1050 is 1 and downshift is 0.

Parity is added by the CCM in the 2^8 bit position.

(Example is the letter D)

B	A	C	8	4	2	1 - IBM bit designations
2^0	2^1	2^6	2^2	2^3	2^4	2^5
1	1	0	0	1	0	0

Received from the line as:

B	A	8	4	2	1	C
2^0	2^1	2^2	2^3	2^4	2^5	2^6
1	1	0	1	0	0	0

SEQUENTIAL MODIFICATION OF IBM 1050 CODE (Cont'd)

CCM modifies character as follows adding shift status and odd parity:

P	S	C	1	2	4	8	A	B
2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	1	0	0	0	1	0	1	1

SEQUENTIAL MODIFICATION OF TYPE 2 DATA SPEED BAUDOT CODE TRANSMISSION

◆ When receiving Baudot (5-level) code from a Data Speed (Type 2). transmitter, each character is received from the communication line in an 8-level code without parity. The 2^0 bit always is spacing 0 and the 2^6 and 2^7 bits always are marking 1 when received from the communication line.

The 2^7 bit indicates shift status. This bit remains 1 if the last previous shift character was Figs, and will be changed to 0 by the CCM if the previous shift character was Ltrs. The 2^6 bit will also be changed to 0 by the CCM.

Therefore, the 2^0 and 2^6 bits are always 0 when entering the CCM. A parity bit is provided by the CCM in the 9th level (2^8) to produce the correct odd parity for the character. See Example (3) below.

(Example is the letter D)

2^5	2^4	2^3	2^2	2^1	
0	1	0	0	1	(Baudot Code)

Received from the line as:

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	1	0	1	0	0	1	0

CCM modifies character as follows, add shift status and odd parity:

P	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	0	0	0	1	0	0	1	0

The framing bits of each asynchronous character are deleted when receiving and inserted when transmitting. The shift characters are deleted by OW action if desired when receiving, but are automatically generated when transmitting.

SEQUENTIAL MODIFICATION OF TELETYPEWRITER BAUDOT CODE TRANSMISSION

◆ The Baudot (5-level) code received from a telegraph circuit, is configured as a 5-level code without parity.

The code is expanded by the CCM to a 9-level code with the 2^7 bit set to indicate shift status. This bit is a 1 if the last previous shift character was Figs, and a 0 if the previous shift character was Ltrs.

SEQUENTIAL MODIFICATION OF TELETYPEWRITER BAUDOT CODE TRANSMISSION (Cont'd)

Expansion of the teletypewriter Baudot code places 0 in the 2^5 and 2^6 bit positions and correct parity is generated in the 9th level (2^8).

(Example is the letter D)

2^5	2^4	2^3	2^2	2^1	(Baudot Code)
0	1	0	0	1	

Received from the line as:

2^5	2^4	2^3	2^2	2^1
0	1	0	0	1

CCM modifies the character as follows adding shift status and odd parity.

P	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	0	0	0	1	0	0	1	0

The framing bits of each asynchronous character, are deleted when receiving and inserted when transmitting. The shift characters, are deleted by OW action if desired when receiving, but are automatically generated when transmitting.

SYSTEM FUNCTIONAL CAPABILITY

- See table 3-3.

SCHEMATIC APPEARANCE OF CCM MEMORY LAYOUT

- See figure 3-1.

LINE STATUS WORDS

- See figure 3-2 and table 3-4.

OPERATIONAL WORDS

- See tables 3-5 and 3-6.

COMMUNICATION REPORTING BYTE

- See table 3-7.

Table 3-3. Remote System Functional Capability

Remote Devices & Systems		Buffer Transmission Characters				Communication Facilities	
System Classif.	Description	Model	Characters per Second	Bits per Second	Bits per Char.(*)	Data Set	Services (See page 3-9)
C_7 C_0							
AT&T Model 28 TTY							
XXXX1000	Point-to-Point (↑H↓)	710	6, 7.5 or 10	45.5, 56.9 or 75	7.5 (5)	None	PTL
XXXX1000	Point-to-Point (NNNN)						
XXXX1000	Selective Calling						
XXXX1000	AT&T 83, B2, B3						
AT&T Model 32 TTY							
XXXX1000	Point-to-Point	710	6 or 10	45.5 or 75	7.5 (5)	None	LL
AT&T Model 33 TTY							
XXXX1110	Point-to-Point	710	10	110	11 (8)	None	LL
XXXX1110	TWX	720-11				Self-contained	TWX
AT&T Model 35 TTY							
XXXX1110	Point-to-Point	710 / 720-21	10	110	11 (8)	None / Self-contained	PTL / 150
XXXX1110	Selective Calling						
XXXX1110	AT&T 8A1 System	720-21				Self-contained	150
XXXX1110	TWX	720-11				Self-contained	TWX
Bell Data Speed, Type II							
XX010110	8 Level, no parity, USASCII	720-21	105	1050	10 (8)	202C / 202D	VMN / PVL
XX110110	8 Level, even parity, USASCII	720-22					
XXXX0100	5 Level, baudot	720-21					

Table 3-3. Remote System Functional Capability (Cont'd)

Remote Devices & Systems		Buffer Transmission Characteristics				Communications Facilities	
System Classif.	Description	Model	Characters per Second	Bits per Second	Bits per Char.(*)	Data Set	Services (See page 3-9)
IBM Data Comm. Systems & Terminals							
XXX00010	1050	710	8.3	75		None	None
XXX00010	1050	720-21	14.8	134.4	9 (7)	103A / Self-contained	VMN / 150
XXX00010	2741	720-23					
IBM Synchronous Transmitter-Receivers							
X0111101	1013 Card XMN Term 2701 Data Adapt. 1009 Data XMX Unit 2073 Communications Adapter	722	250 / 75 or 150 / 75 or 150 / 300	2000 / 600 or 1200 / 600 or 1200 / 2400	8 (8)	201A4 / 202C / 202D / 201B2	VMN / PVL
RCA Display Devices							
XX110110	6050-11, 12, 13 VDT	720-21	105 or 120 / 105, 120, or 180	1050 or 1200 / 1050, 1200, or 1800	10 (8)	202C / 202D	VMN / PVL
	6077 Interr. Control Term.	720-21					
XX111110	6050-21, 22, 23 VDT	720-21	10	110	11 (8)	103A	VMN
						103F	150
XX110110	70/752 Video Data Terminal	720-21	120	1200	10 (8)	202C / 202D	VMN / PVL

Table 3-3. Remote System Functional Capability (Cont'd)

Remote Devices & Systems		Buffer Transmission Characteristics				Communications Facilities	
System Classif.	Description	Model	Characters per Second	Bits per Second	Bits per Char.(*)	DATA SET	Services (See page 3-9)
RCA Data Collection System							
XX000110	70/630 DGS (Long Distance)		720-22	120	1200	10(8) 202D	PVL
XXX01101	70/630 DGS (Local)		725	120	960	8 None	
X0010010	6201 EDGE		724	27.7	250	9(7) None	
RCA 301/3301 Communication Buffers and Controls							
X1100101	6012 376 3376	721	250 / 300	2000 / 2400	8(7)	201A3 / 201B1	VMN / PVL
RCA Remote Terminals							
XXX00101	70/740 Remote Printer Term.	721	250 / 300	2000 / 2400	8	201A3 / 201B1	VMN / PVL
XXX01010	5925 Communications Term.	720-22	15	150	10(7)	103A / 103F / Self-Contained	VMN / PVL / 150
RCA Voice Response Unit							
XX011101	70/510 VRU	715	-	8 (Parallel)		X403A	VMN

Table 3-3. Remote System Functional Capability (Cont'd)

Remote Devices & Systems		Buffer Transmission Characteristics				Communications Facilities	
System Classif.	Description	Model	Characters per Second	Bits per Second	Bits per Char.(*)	Data Set	Services (See page 3-9)
RCA Spectra 70 Communication Buffers and Controls							
X0100101	70/653 (8 Level)	721	250 / 300	2000	8 (8)	201A3	VMN
X0100101	70/721 (8 Level)						
XX100111	70/653 (9 Level)		222 / 267	2400	9 (9)	201B1	PVL
X0100111	70/721						
X01001f0	70/720-21	720-21	120	1200	10 (8)	201C/202D	VMN/PVL
XX000111	70/780 Time Generator	Self-Contained CCM Sel Rate			9 (9)	None	None
UNIVAC Data Line Terminals							
XXX01001	Type I - Univac DCT-2000	721	286	2000	7 (7)	201A3	VMN
			343	2400		201B1	PLL

X in system classification indicates programmer option to differentiate between similar systems. Bit C_7 controls timer; if $C_7 = 1$, timer is activated, if $C_7 = 0$, timer is off.

*Data bits per character, including parity if used.

Services Legend

LL - Customer-Owned or leased, on-premises, local
PTL - Private Telegraph Line
TWX - Teletypewriter Exchange Network
VMN - Voice Message Network
PVL - Private Voice-grade Line
150 - 150 baud line

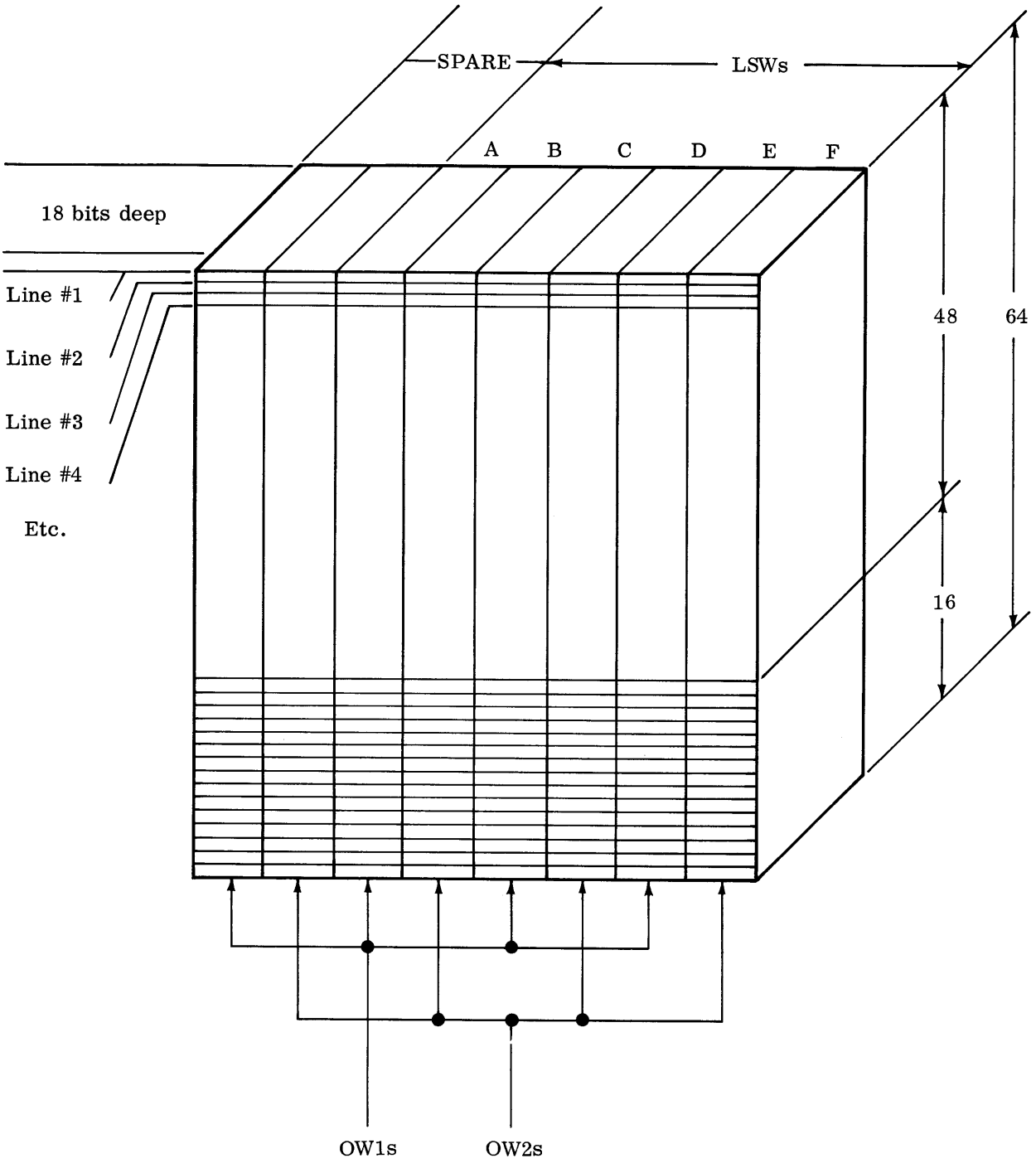
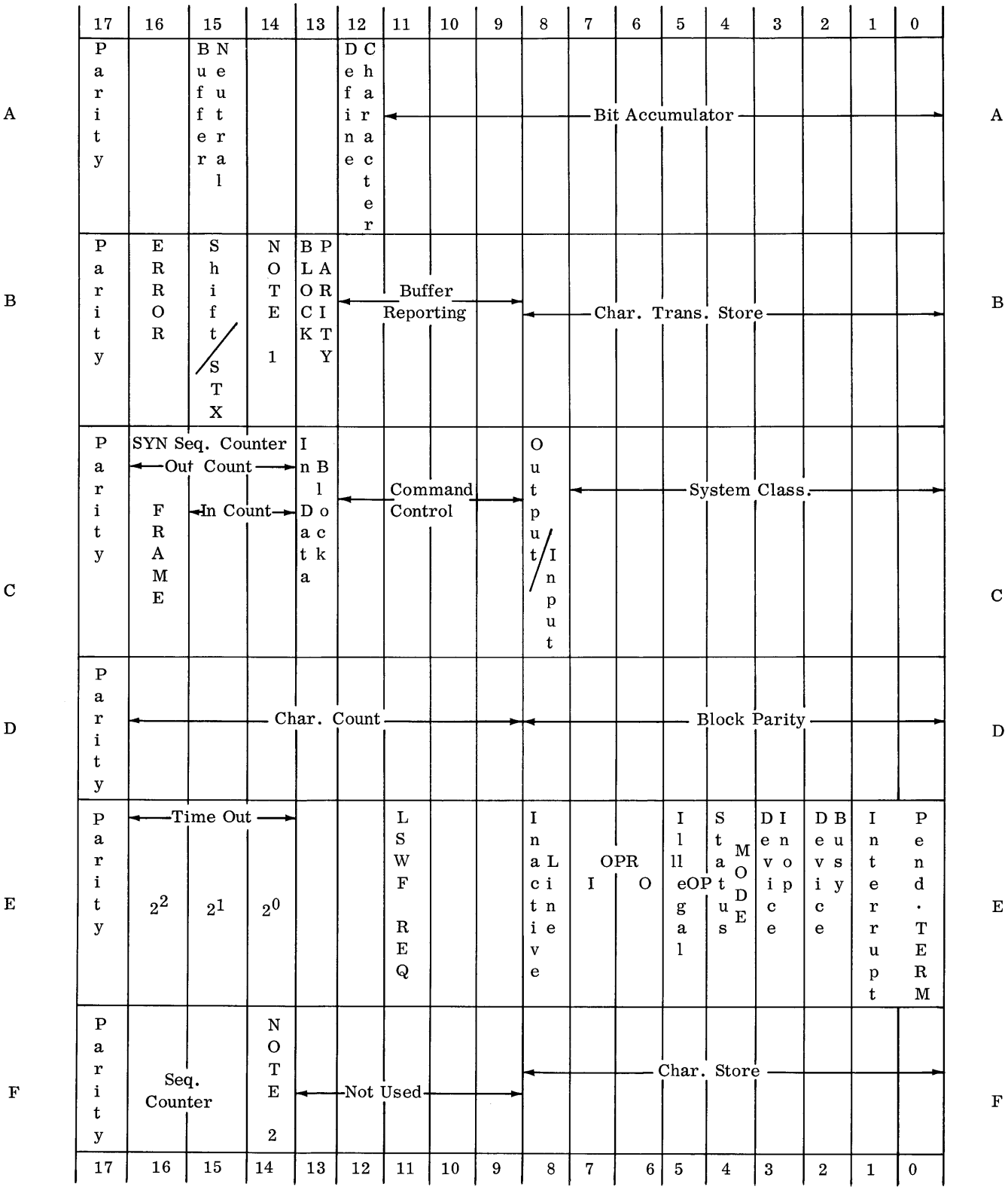


Figure 3-1. Schematic Appearance of CCM Memory Layout



Notes -

1. (B 14) Character Transfer Control
2. (F 14) Special Control

Figure 3-2. Line Status Words Layout

Table 3-4. Line Status Words (LSW)

Item Description	Bit Assign	Function	Operation
Bit accumulator/ distributor	A0 to A11	Character assembly and serializing.	Incremented by bit transfer to/from buffer and character transfer store. Accommodates codes having a maximum of 11 bits, including framing bits, as specified by systems classification. LSWA 11 is used for control bit when 11 bit code is used.
Define character	A12	Synchronization detection and control.	Enable transfers between character transfer store and bit accumulator/ distributor.
Not Used	A13, A14		
Buffer neutral	A15	Buffer neutral status recording.	Set when buffer receives Term. Reset when command initiated.
Not Used	A16		
Parity	A17		
Character transfer store	B0 to B8	Character storage between processor and bit accumulator/ distributor.	
Buffer reporting	B9 to B12	Buffer report storage.	Used for generation of coordination message.
Block parity	B13	Indication that next character is block parity.	Set by operational word - Reset by block parity character.
Output character from memory	B14	Character transfer control. Controls transfer of character from character transfer store to bit accumulator/distributor.	Set and reset by hardware.

Table 3-4. Line Status Words (LSW) *(Cont'd)*

Item Description	Bit Assign	Function	Operation
Shift	B15	Shift status indication.	Compared with data to determine appropriate action: 0 - upper case; 1 - lower case. Set and reset by CCM logic. Reset by hardware upon the issuance of a Read, Write, or Write Control except during Read to Read command chaining for systems using message separation.
Error	B16	Error recording.	Set on input/output parity error or improper character framing. Set when reported by coordination message.
Parity	B17		
System classification	C0 to C7	Communication system indication.	Initialized by program.
Input/output	C8	Buffer command status recording.	Set on Write or Write Control command. Reset on read command. Indicates that last command sent to buffer was a Write or a Read.
Command control	C9 to C12	Command storage.	Set by processor command or operational word. Reset when transmitted to the buffer.
In data block	C13	Noise protection and synchronization.	Qualifies action taken on character recognition, and when set, permits character to be transferred to the processor. Set and reset by operational word and reset by command initiation, where specified, in terms of applicable system classification.

Table 3-4. Line Status Words (LSW) *(Cont'd)*

Item Description	Bit Assign	Function	Operation
SYN sequence counter	C14 to C16	Line synchronization establishment and maintenance.	Used to generate appropriate number of SYN characters when initiating synchronous transmission and permits counting of incoming SYN characters to establish synchronization when receiving.
Parity	C17		
Block parity	D0 toD 8	Accumulated block parity character storage.	Binary add without carry of each character.
Character counter	D9 to D16	Character count.	Incremented on each character to or from processor.
Parity	D17		
Interrupt pending	E0 to E1	Pending termination interrupt or PCI indication.	Set by SET INT command or lead from MPX channel. Reset when interrupt reported.
Standard Device byte	E2 to E5	Assembly of standard device byte.	
Line operation (Buffer is input/output)	E6, E7	Buffer (line) command status.	Set on receipt of Write, Write Control, or Read command from processor. Reset on END. E7 E6 0 0 Quiescent 0 1 Read Command 1 0 Write Command 1 1 Write Control
Inactive line	E8	Indicates when device address not occupied or buffer cannot accept any commands.	Set to 1 by program for all inactive device addresses at initialization. An address (command) sent to a device address with this bit set is ignored (Ready is not returned by the CCM).

Table 3-4. Line Status Words (LSW)(Cont'd)

Item Description	Bit Assign	Function	Operation
Not used	E9, E10		
LSW F required	E11	Indicates that LSW F contains additional CCM action requirements.	Set by hardware to indicate character is present in LSW F character store area. Reset when character is removed.
Not used	E12, E13		
Time out counter	E14 to E16	Permits generation of CM at timeout interval. (Nominally 20 seconds).	See Data Timeout Description.
Parity	E17		
Character store	F0 to F8	Receive: Previous Character comparison storage. Transmit: Temporary storage of data character which is preceded by a hardware generated shift character.	Stored under control of Operational Word and as a result of comparison of 2^7 bit of character and shift bit, B15.
Not Used	F9 to F13		
Special control	F14	Modify OW address (refer to bit 4 of OW-2.)	Set and reset by operational word according to system requirement. A character is normally used as a control character. If a given character is also used as SOM, in a system using block parity, F14 would be set upon recognition of SOM. This would prevent that character from being recognized as SOM until this condition was reset by EOM. Therefore, should the SOM character appear in

Table 3-4. Line Status Words (LSW) (Cont'd)

Item Description	Bit Assign	Function	Operation
Special control (Cont'd.)			the text of the message it would be considered a data character and not as a control character.
Sequence counter	F15 to F16	Multicharacter control sequence counting.	Set or triggered by operational word. Reset by operational word or non-control character transfer.
Parity	F17		

Table 3-5. Operational Words OW-1

Bit	CCM Action
2, 1, 0	Action Control bits. These bits establish the conditions under which indicated coordination message or termination action is taken. Following are the assigned bit configurations and their significance: 001 Unconditional action. 010 Action taken only if the character currently in character transfer store is the last of a nonidentical two-character sequence, e.g., AB. 011 Action taken only if the character currently in character transfer store is the last of an alternate nonidentical two-character sequence, e.g., CD. 100 Action taken only if the character currently in character transfer store is the last character of an identical two-character sequence, e.g., AA. 101 Action taken only if the character currently in character transfer store is the last character of an identical four character sequence, e.g., AAAA. 000, 110, 111 Not assigned. Note: Bit settings of 010 and 011 are not normally used, but may be if the loading on the sequence counter is considered excessive. Bit settings 100 and 101 are used so that a single OW need be accessed to control this function.
3	Not used.
4	Set in data block bit in LSW, under control of action control bits.
5	Reset in data block bit in LSW, under control of action control bits.
6	Inhibit sequence counter setting (overrides 000 setting of bits 7, 8.)
8, 7	These bits, along with bit 6, control the sequence counter in the line status word permitting the recognition of the various control sequences described in bits 0-2. 000 Reset sequence counter to 00 (operates only when bit 6 = 0). 001 Set sequence counter to 01 (operates regardless of other bits in connection with nonidentical two-character sequence). 010 Set sequence counter to 10 (operates regardless of other bits in connection with nonidentical two-character sequence). 011 Trigger sequence counter (operates regardless of other bits).

Table 3-5. Operational Words OW-1 (Cont'd)

Bit	CCM Action
8, 7 (Cont'd.)	100 Do nothing 101, 110, 111 Not used Communication Reporting Byte (CRB) Program Notification (See Table 3-7.)
12, 11, 10, 9	If other than 0000 and if permitted by action control bits 0-2, generate a CM with these bits appearing in positions 2^0 -2^3 (CRB). See table 3-7 for specific bit settings.
13	Terminate existing command where permitted by action control bits 0-2.
	The following bits (14, 15, and 16) operate independently of the action control bits.
14	Exclude this character from block parity count. (Applicable only for system calling for block parity as specified in their system classification).
15	Ignore this character (Reset character transfer store to zeros). Inhibit the transmission or reception of that character).
16	OW-2 required.
17	Parity.

Table 3-6. Operational Words OW-2

Bit	CCM Action
0	Reset block parity counter in LSW (D, 0-8).
1	Reset character counter in LSW (D, 9-16).
2	Set next character is block parity bit in LSW (B-13).
3	Set status modifier bit in standard device byte (2^0).
4	Set LSW bit F14. (special control).
5	Reset LSW bit F14.
6	Set LSW bit F12 (not used).
7	Reset LSW bit F12 (not used).
8	Set LSW bit F11 (not used).
9	Reset LSW bit F11 (not used).

Table 3-6. Operational Words OW-2 *(Cont'd)*

Bit	CCM Action
11, 10	Not used.
13, 12	Special buffer control: 2^{13} 2^{12} 0 0 No action. 1 0 Generate DISC command to buffer. 0 1 Generate ACK command to buffer if LSW bit B16 is reset. 1 1 Not used.
16, 15, 14	Not used.
17	Parity.

Table 3-7. Communication Reporting Byte (CRB)

Bit Configuration								Meaning
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	
0	0	0	0	0	0	0	0	No CM required.
X	X	X	X	0	0	0	1	Good message.
X	X	X	X	0	0	1	0	Bad message.
X	X	X	X	0	0	1	1	Bits (2^0 - 2^3) are variable by the program and may be set in each operational word to give any desired indication.
			⋮					
X	X	X	X	1	1	1	1	
0	1	0	0	X	X	X	X	Buffer malfunction.
0	1	0	1	X	X	X	X	Overlay - character received from buffer before previous character transferred to the processor.
0	1	1	0	X	X	X	X	Optional buffer report 1 (LDR for 70/715 Parallel Buffer.)
1	0	1	0	X	X	X	X	Buffer error.
1	1	0	1	X	X	X	X	Ring report.
1	1	1	1	X	X	X	X	Time-out.
0	1	1	1	X	X	X	X	Optional buffer report 2.
								Set by operational word.
								Set by buffer report.

PHYSICAL CHARACTERISTICS

◆ The CCM consists of the following subunits:

Cabinet

Control Electronics

Control Panel

Maintenance Panel

Signal Termination Boards

Power Supply

Buffers

Buffer Capacity

◆ Depending upon the quantity and type of buffer required for each application, one or the other of two types of CCM cabinets is supplied. Future requirements must be considered prior to installation, since field conversion from one type to the other is not possible.

Type I - provides up to 3 10-block rows and 16 9-block rows for buffers.

Type II- provides up to 16 10-block rows and 32 9-block rows for buffers. This type is provided only when required for CCM Models 70/668-21 and 31.

Where buffer dimensions permit, several buffers can be located in one CCM plug-in row. However, each must occupy a contiguous space. Space left in a row which is not sufficient to accommodate a buffer can be used for buffer special features. However, a buffer special feature must be adjacent to the buffer in the same row or in a row immediately above or below that buffer. Buffers which occupy more than one row must occupy adjacent rows in the same area.

Line Terminal Board

◆ The Line terminal board is located at the bottom of the left end of the cabinet and is accessible through the doors provides fixed terminations for lines which employ current (telegraph-type) interfaces. Provision is made for installation of 48 telegraph line filters provided with various buffers.

Overall Cabinet Dimensions

	Type I	Type II
Height:	62"	62"
Width:	54-5/8"	104-1/4"
Depth:	24-3/4"	24-3/4"

Weight (Without Buffers)

Type I: 1090 lbs.
Type II: 1793 lbs.

Buffer Identification

◆ Provision is made to identify the buffers on the buffer or in the CCM rack. This identification is performed in such a manner that additions and or changes may be made. The buffer identification provides information such as the following:

1. Buffer type.
2. Buffer serial number.
3. Common carrier facilities, including grade of service, line number and location(s) served by the line.
4. SEL number being used.

Controls and Indicators

◆ Control Panel

The following operator controls and indicators for the CCM and buffers are located on the Control Panel:

Power On/Off (switch indicator) - Applies or removes input power to the CCM logic and buffers. The indicator lights when power to the logic is on.

On Line (indicator) - Indicates that the CCM is connected to the multiplexor channel permitting signal exchange on the standard I/0 interface.

Buffer Scan (indicator) - Indicates that the line scan is advancing.

Processor Scan (indicator) - Indicates that the processor (SR) scan is advancing.

Interrupt Scan (indicator) - Indicates that the interrupt scan is advancing.

Buffer Status (48 numbered, independent indicators) - Indicates that a mark or 1 is being exchanged with a remote device by the respective buffer.

Features

Feature 5618 - USASCII Block Check Character

◆ This feature modifies the block parity operation of the CCM to conform to the proposed standard as defined by the United States of American Standard Code for Information Interchange (USASCII). When installed, it is effective for all lines whose system classifications identify them as using USASCII. The handling of block parity with non-USASCII systems is not affected.

The block check character (BCC) for USASCII systems is accumulated by taking a binary sum independently on each of the seven individual levels (b1-b7) of the transmitted or received code. The correct value of the parity bit of the BCC is generated when transmitting and tested when receiving. The correct value of the parity bit is defined as that which makes the parity sense of the BCC the same as for the text characters.

Feature 5617-1
TELEX Operation

◆ This feature enables the CCM to operate with Western Union TELEX, through the 70/710 Telegraph Buffer. TELEX is a switched network service operating at 6.6 characters per second. This feature provides an alternate oscillator which generates the 50-bit-per-second modulation rate necessary for TELEX. The oscillator set provided with this feature can be accommodated only in the location normally occupied by either set No. 2 or set No. 3.

4. COMMUNICATION BUFFERS

◆ The various Spectra 70 buffers interface both the CCM and the communication line facilities serving as the send and receive pathways over which data is exchanged between the CCM and the remote terminals which it services.

The buffers accept and present data to and from the communication lines serially, a bit at a time. In order to assure a orderly flow of data in both directions, the CCM and the buffers exchange the data and appropriate control signals in a logical sequence similar to that exchanged between the CCM and the processor.

CCM - BUFFER SIGNAL SEQUENCE

◆ A buffer is serviced when the buffer scan arrives at the line to which its Select (SEL) lead is connected. The sequence is as follows:

SELECT

◆ The CCM generates a SEL signal on a line which is unique for a designated buffer.

BUFFER RESPONSES

◆ The buffer responds with its status signals and data level as follows:

Buffer Operable (BOP)

◆ Indicates that the scan position is occupied and that the buffer is operable. If buffer responds with Inoperable, any command present is terminated and bit 2^1 (device inoperable) is set in the standard device byte, thus suppressing any chaining.

Ready (RDY)

◆ Enabled only when a Receive, Transmit, or Auto-Call command is present in the buffer. It indicates that the buffer is ready to transmit a bit to the CCM or to receive a bit from the CCM.

Reports

◆ The buffer reports specific conditions to the CCM by encoding the RPT 1, 2, 3, signals.

Data:

A bit is present when the buffer is Ready during Receive. The CCM must accomplish the transfer prior to dropping SEL.

CCM RESPONSES

◆ The CCM responds to the foregoing with command signals, control signals, and data level as follows:

1. *Commands*- The CCM issues specific commands to the buffer by encoding the COM 1, 2, 3 signals.

2. *Strobe* (STB) - Data is accepted from the buffer, and data and commands are transferred to the buffer by means of the STB signal.

3. *Report Acknowledged* (RAK) - The CCM acknowledges action taken on Reports. This response permits the buffer to change RPT signals.

Transmit Data:

A bit is presented to the buffer after the buffer has indicated RDY during Transmit. The CCM must present the bit during SEL when RDY is indicated by the buffer.

Commands

◆ The CCM encodes the COM 1, 2, and 3 signals to the buffer to accomplish the following buffer functions.

Disconnect (DISC)

◆ This command causes the buffers to break an existing line connection. DISC results from a Disconnect Write Control or Operational Word. (See tables 3-5 and 3-6.)

Transmit (TC)

◆ This command conditions a buffer for transmission. TC results from a Write command or a Suppress Start/Stop Write Control command.

Receive (RC)

◆ This command conditions a buffer to receive data. RC results only from a Read Forward command.

Auto-Call (ACC)

◆ This command enables buffers with auto-call capability to transfer dialing digits to an automatic calling unit where applicable. ACC results only from an Auto-Call Write Control command.

Acknowledge (ACKC)

◆ This command causes certain buffers to generate and transmit a timed acknowledgement signal. ACKC results from an acknowledge Write Control or operational word.

End Character (ECC)

◆ This command is controlled by systems classification and is presented along with the last signal element of each character when transmitting (asynchronous systems) and during the SEL interval in which the next to the last signal element is transferred to the CCM when receiving (synchronous systems). This command is spontaneously generated by the CCM as a result of its character serializing and assembly functions during the buffer scan. If any other command is to be issued during the same SEL interval, the ECC is surpressed. The ECC does not cause the buffer to change its command state.

At the present time, the ECC is applicable to only the 70/722 Synchronous Transmitter Receiver Buffer during receiving and the 70/720-11 Asynchronous Data Set Buffer when transmitting (TWX applications).

Terminate (TERC)

◆ This command, which is presented with the last bit when transmitting, or at any time when receiving, causes the buffer to conclude the operation specified by the previous command and to respond to SEL with END when it can accept a new command. TERC results from command termination or operational word.

Command Signals

◆ The bit configurations of the COM 1, 2, and 3 signals from the CCM to buffers are:

Out of Service (OSC) (70/715 Parallel Buffer)

The function of an OSC is to condition the data set to appear out of service or busy to an incoming call. This command requires that DTR to the data set be off.

Call Attendent (CAC) (70/715 Parallel Buffer)

A CAC causes the buffer to signal for attendent intervention on any particular call. This command requires that DTR to the data set be one.

Command Signals *(Cont'd)*

Auto-Call, Acknowledge, and Disconnect Commands are issued as a result of Write Control commands from the processor.

COM 3	COM 2	COM 1	Command or Condition
0	0	0	Quiescent
0	0	1	Transmit (TC)
0	1	0	Receive (RC)
0	1	1	End of Character (ECC)
1	0	0	Terminate (TERC)
1	0	1	Auto-Call (ACC)
1	1	0	Disconnect (DISC)
1	1	1	Acknowledge (ACK)
1	0	1	Out of Service (OSC)
1	0	1	Call Attendent (CAC)

REPORTS

◆ The CCM decodes the RPT 1, 2, and 3 signals from the buffer to determine the following:

Malfunction (MR)

◆ This report is permitted only when a Transmit, Receive, or Auto-Call command is present in the buffer. It indicates an improper line or communication hardware condition of a permanent nature, and causes the CCM to terminate the command. Bit 2^1 (device inoperable) is set in the standard device byte, suppressing any chaining, and a coordination message is generated. When this condition occurs coincident with error, only the MR is reported to the buffer.

Error (ER)

◆ This report is permitted only when a Transmit, Receive, or Auto-Call command is present in the buffer. It indicates an improper line or communication hardware condition of a transient nature. Such conditions are reported by the buffer once per occurrence. When errors are reported, a coordination message is generated.

Line Disconnect Report (LDR)

◆ When a Transmit or Receive command is present and prior to END, the Parallel Buffer, Model 70/715, indicates a remote disconnect condition to the CCM via an LDR.

Ring (RR)

◆ This report is not affected by the command status of the buffer. It indicates that ringing is occurring on the line to which the buffer is connected. Each ringing burst is reported once by the buffer. Ring is normally present only where the buffer interfaces a communication termination on a switched network application. With the 70/715 Buffer, RR is permitted only when the buffer is in the quiescent state.

End

◆ This report is permitted by TERC, DISC, or ACKC commands. It indicates that all buffer action in connection with the terminated command has been completed. A new command can be accepted by the buffer after END has been reported.

Error and End

◆ This report indicates that ER and END conditions as previously indicated have occurred since the previous SEL to the particular buffer.

Optional

◆ These reports indicate a condition unique to a particular buffer which is to be reported to the program in a coordination message. No action other than the generation of the coordination message is performed by the CCM.

RPT 3	RPT 2	RPT 1	Report or Condition
0	0	0	Quiescent
0	0	1	End
0	1	0	Error
0	1	1	End and Error
1	0	0	Malfunction
1	0	1	Ring
1	1	0	Optional 1 (LDR, BDR*)
1	1	1	Optional 2

*Break Disconnect Report - 70/720-22.

CAUSES OF MR, ER, AND LDR REPORTS

◆ Malfunction, Error, and Line Disconnect Reports are reported to the CCM by the buffers as a result of certain detected conditions normally related to the communication line, the data set, or the automatic calling unit. The following is a list of the reports generated to the various buffers depending upon the abnormal conditions present:

Buffer	Report	Command	Condition Reported
70/710	MR	TC	Bit-echo check failure.
70/715	MR	TC	Loss of DOP from VRU.
	ER	TC	Presence of data in 70/715 at the end of a WT pulse.
	LDR	TC	Absence or loss of DSR.
	LDR	RC	Loss of DSR.
70/720-11,21	MR	TC	Loss of DSR.
		RC	Loss of DSR.
	ER	TC	Loss of RD or SRD.
		RC	Loss of DCD.
70/720-22	MR	TC	Loss of DSR.
	MR	RC	Loss of DSR.
	ER	TC	Loss of CTS.

CAUSES OF MR, ER, AND LDR REPORTS (Cont'd)

Buffer	Report	Command	Condition Reported
70/720-22 (Cont'd)	ER	RC	Loss of DCD.
	BDR	TC	Loss of RD or SRD. (Absence of signal on reverse channel.)
70/720-23 (same as 70/720-22, except for the following)			
	EER	TC	14ms. of spacing on RD.
	BDR	TC	140ms. of spacing on RD.
70/721	MR	TC	Loss of DSR.
		RC	Loss of DSR.
	ER	TC	Loss of CTS.
		RC	Loss of DCD.
70/722	MR	TC	Loss of CTS or DSR.
		RC	Loss of DSR.
	ER	TC	Not used.
		RC	Loss of DCD.
70/724	ER	RC	Loss of carrier.
70/725	MR	RC	Absence of carrier for more than 1000 ms.
			Presence of ACK, NAK or RT (Request to Transmit) for more than 1000ms.
		TC	Absence of carrier for more than 1000ms.
	EER	RC	Interruption of carrier for 3ms. or more.

Causes of MR and ER Reports When Using Automatic Calling Units

Buffer	Report	Command	Condition Reported
70/720-11,21	MR	ACC	Loss of PWI.
	ER	ACC	Receipt of DLO or ACR.
70/721	MR	ACC	Loss of PWI.
	ER	ACC	Receipt of DLO or ACR.

DATA SET, ACU, AND VRU SIGNAL REFERENCE LIST

◆ The following is an identification list of the interface signals associated with the buffers and auto-call special features. These signals are relevant only to those buffers which interface common carrier data sets: 70/715, 70/720, 70/721 and 70/722.

Data Set to Buffer

◆ DSR - Data Set Ready - Generated by the data set when in the data mode.

CTS - Clear to Send - Data set is ready to transmit data.

DCD - Data Carrier Detect - Indicates transmission carrier is ON.

RD - Received Data - Indicates presence of incoming data.

SRD - Supervisory Received Data - (70/720-22) indicates presence of data on reverse channel from remote.

RI - Ring Indicator - Indicates presence of incoming call on switched network applications.

RDT - Restraint Detected - (70/720-11) used with TWX applications to indicate that processor must hold off transmission for a short time.

SCT - Serial Clock Transmitter (70/721) - Signal from data set which establishes bit timing of transmission.

SCR - Serial Clock Receiver (70/721) - Signal from data set derived from the synchronization established by a similar remote data set. SCR works in conjunction with SCT to provide the proper transmission synchronization.

Buffer to Data Set

◆ DTR - Data Terminal Ready - Permits data set to enter and remain in data mode during transmission.

RS - Request to Send - Indicates to data set that buffer has data to Transmit.

TD - Transmit Data - Presents transmitted data to data set.

STD - Supervisory Transmitted Data - Limits the transmit and receive data in using reverse channel applications.

EDT - EOT Detected (70/720-11) - Used in TWX applications to disconnect data set after processor recognizes EOT.

NS - New Sync - (70/72) Used to establish a more rapid synchronization transition in multistation applications.

SCTE - Serial Clock Transmitter External (70/721) Used when bit timing is derived from buffer rather than data set as is the case in most applications where this buffer is used.

Automatic Calling Unit to Special Feature

- PWI - Power Indication - Indicates ACU has power from power source.

DLO - Data Line Occupied - Presents indications whenever communication line associated with ACU is in use.

PND - Present Next Digit - Indicates the ACU is ready to accept a dialing digit from the processor.

DSS - Data Set Status - This signal is present when the associated data set is in the data mode.

ACR - Abandon Call and Retry - Indication from ACU that a desired event in the calling procedure has not occurred within a preset time.

Special Feature to Automatic Calling Unit

- CRQ - Call Request - Indicates that the processor is initiating a call.

DPR - Digit Present - Indicates that the special feature digit leads may be read by the ACU.

Voice Response Unit to Parallel Buffer

- DOP - Device Operable - Generated by VRU when it is capable of voice response.

WT - Word Time - Generated by VRU when it is able to accept a new word address.

The following list indicates the block size of the product line Spectra Buffers and Special Features which can be used with specific buffers. Knowledge of block size is helpful in determining the physical hardware requirements of a system and for selecting the proper buffer rack size.

Buffer	Block Size	Special Features	
		Automatic Calling	Full Duplex
70/710	3	-	-
70/715	7	-	-
70/720-11	5	2	-
70/720-21	4	2	1
70/720-22	5	-	-
70/720-23	4	-	-
70/721	4	2	1
70/722	10	-	-
70/724	5	-	-
70/725*	9	-	-
70/780	14	-	-

*The 70/725 is a dual buffer assembled as one unit. The above list indicates total block size of both units.

TELEGRAPH BUFFER (TB) MODEL 70/710

GENERAL DESCRIPTION

◆ The RCA Model 70/710 Telegraph Buffer (TB) operates asynchronously with 62.5 ma. 130 volt, neutral telegraph circuits. It is compatible with both private line telegraph circuits leased from a common carrier, or equivalent customer provided facilities. The Telegraph Buffer is used with the Communication Controller - Multichannel (CCM), Model 70/668, and occupies one scan position of the CCM when operating with half-duplex circuits. Two telegraph buffers and two scan positions of the CCM must be used when operating with full duplex facilities.

REMOTE DEVICES AND SYSTEMS

◆ The buffer operates with the following telegraph terminal devices and systems:

Model 28 Teletypewriter Equipment associated with private line point-to-point or multipoint configurations. This includes common carrier teletypewriter systems capable of polling, selective calling, answer-back, and other common operational features.

Models 32 and 33 Teletypewriter Equipment used on point-to-point communications facilities with systems where these remotes as well as the controlling processor are located on the same premises. Selective calling is not available with this equipment.

Model 35 Teletypewriter Equipment used on communication facilities with systems where these devices as well as the controlling processor are located on the same premises.

OPERATIONAL CHARACTERISTICS

◆ The 70/710 Telegraph Buffer exchanges data in bit serial between the communications line and the CCM. The buffer transfers the data bits in each direction without altering their sense or order (1 or 0). The buffer is controlled by the CCM which initiates commands to the buffer to place it in the proper operational mode.

Commands

◆ The Command signals from the CCM are decoded by the buffer into the following commands:

Transmit (TC) and Terminate (TERC)

The TC and TERC commands condition the telegraph buffer for data transmission.

Receive (RC) and Terminate (TERC)

The RC and TERC commands condition the buffer for data reception.

Data Transfer

Initial Conditions

◆ Whenever the buffer receives a SEL from the CCM, it responds with BOP regardless of command status or line condition. In the absence of a command, the buffer remains in the condition in which it was placed upon termination of the previous command. It is then conditioned to receive a new command.

Whenever a signal appears on the Reset lead from the CCM, the buffer is restored to its quiescent condition and the command which was present, if any, is dropped. The buffer responds to subsequent SELs with BOP only until another command is received.

Transmit

◆ The telegraph buffer executes a TC as indicated and responds to a CCM SEL with RDY. A bit is received from the CCM on the data lead. It is transferred to bit storage and then to the line with the same sense (1 or 0) as received from the CCM. Thereafter, the buffer becomes RDY and transfers the second bit to storage. By means of bit timing which the telegraph buffer derives from a CCM oscillator, the second bit is transferred to the line at the proper time. Subsequent bits are transferred to the line in the same manner. When TERC is received along with the last bit to be transmitted, the buffer applies the bit to the line and terminates as previously indicated.

Note:

The buffer places a marking (1) bit on the line unless a spacing (0) bit is made available by the CCM.

Receive

◆ The buffer executes an RC as previously indicated and is conditioned to detect a spacing (mark-to-space transition) condition on the line. After detecting a spacing condition, by means of a bit timing which the buffer derives from a CCM oscillator; a bit is transferred to storage. The buffer responds to a CCM SEL with RDY. The bit is transferred to the CCM on the Data lead with the same sense (1 or 0) as received from the line. Subsequently, bits are transferred from the line to storage and then to the CCM until TERC is received. Thereafter, the buffer inhibits RDY and terminates as previously indicated.

Note:

Bit timing is restarted on each mark-to-space transition.

Reports

◆ The Report signals to the CCM are encoded by the buffer to show the following conditions:

Malfunction (MR) END

Malfunction (MR)

◆ When a TC is present, but after an RDY and prior to END, the buffer indicates a malfunction condition to the CCM via a Malfunction Report (MR) upon detection of a failure of the "bit-echo" check.

After an MR, upon receipt of RAK from the CCM, the buffer terminates the command and does not report END to the CCM. The buffer is then in the quiescent condition.

END

◆ The buffer reports END whenever it completes the operations required by each command as previously indicated. END is enabled only by a TERC from the CCM.

Line Termination

◆ The buffer is connected to the CCM line termination panel where telegraph lines are terminated. Telegraph line filters are supplied with the buffer for installation on the line termination panel.

Speed Selection

◆ The buffer must be connected to the proper modulation rate oscillator in the CCM at the time of installation . Speed selection is based upon the type of communication facility connected to the buffer and the requirements of the remote terminal(s). The buffer operates at the transmission speeds and modulation rates as shown in table 4-1 according to the type of remote terminal it is exchanging data with.

Table 4-1. Model 70/710 Remote Device Characteristics

Teletypewriter Terminals	Code Level	Characters per Second	Bits per Second (Modulation Rate)
Model 28	5	6, 7.5, 10	45.5, 56.9, 75
Model 32	5	6, 10	45.5, 75
Model 33	8	10	110
Model 35	8	10	110

Controls and Indicators

◆ The operator controls and indicators for the buffer are located on the CCM control panel. They consist of the following:

Data (amber indicator) - With a TC present, this indicator lights except when a spacing bit is transmitted. With an RC present, after the first mark to space transition, this indicator lights except when a spacing bit is received.

Select (patch panel) - The buffer is easily connected to any CCM Select (SEL) line, and is thereby enabled with power is on. When the buffer is enabled, it responds to an SEL with BOP.

PARALLEL BUFFER (PB), MODEL 70/715

GENERAL DESCRIPTION

◆ The RCA Model 70/715 Parallel Buffer (PB) occupies one scan position on the Communications Controller Multichannel (CCM), Model 70/668, and permits it to receive bit-parallel data from an AT&T 403A data set, or equivalent transfer track addresses to a Voice Response Unit (VRU), Model 70/510, or modulate an Answer Back tone to the calling party. The maximum character transfer rate from the data set is 10 characters per second. The address transfer to the VRU occurs once every 0.533 seconds. Data transfer between the CCM and the buffer is bit-serial at the Select rate.

OPERATIONAL CHARACTERISTICS

◆ Control signals and data bits are exchanged between the buffer and the CCM in a prescribed sequence:

1. CCM selects the buffer.
2. The buffer presents its status signals and data level.
3. CCM issues command signals and a data level.
4. CCM drops Select, allowing the buffer to change its status signals and data level.

Signals and data levels are accepted by the buffer and CCM at strobe time. RAK permits the buffer to change its report status.

Commands

◆ The command signals from the CCM are decoded by the buffer into the following commands:

Command	Bit Configuration 3	2	1
Disconnect (DISC)	1	1	0
Transmit (TC)	0	0	1
Receive (RC)	0	1	0
Out of Service (OSC)	1	0	1
Call Attendent (CAC)	1	0	1
Terminate (TERC)	1	0	0

Disconnect (DISC)

◆ The DISC command restores the buffer and data set to their quiescent conditions; such that the line (trunk) is disconnected. A Ring Report (RR) is permitted only in this quiescent state.

Transmit (TC)

◆ The TC command conditions the buffer to transfer bit-serial track addresses to the VRU or to activate the AB tones.

Receive (RC)

◆ The RC command conditions the buffer and data set for data reception.

Terminate (TERC)

◆ The TERC command conditions the buffer to terminate a transmit, receive, or auto-call command.

Out of Service (OSC)

◆ The OSC command conditions the data set to appear out of service or busy to an incoming call. Upon receipt of an OSC, the buffer turns OS if DTR is off and responds to a SEL with END.

The buffer is restored to service by a DISC. The buffer automatically goes out of service if power fails or upon receipt of the Reset signal from the CCM.

Call Attendent (CAC)

◆ A CAC command causes the buffer to signal an attendent to take a call. DTR must be on in order for the command signal to be interpreted as CAC rather than OSC.

Data Transfer

Initial Conditions

◆ Whenever the buffer receives a SEL from the CCM, it responds with BOP; regardless of command status or line condition. In the absence of a command, the buffer remains in the condition in which it was placed upon termination (END) of the previous command. It is conditioned to receive a new command.

Whenever a signal appears on the Reset lead from the CCM, the buffer is restored to its quiescent condition and the command which was present, if any, is dropped and OS is turned on. The buffer responds to a subsequent SEL with BOP, only; until another command is received.

Receive

◆ The buffer executes an RC as previously indicated. When DP is on, the buffer is conditioned to gate a bit-parallel character (A1 to A4 and B1 to B4) into a register from the data set. The buffer then responds to a CCM SEL with RDY. The stored character is transferred to the CCM on the Data lead, one bit at a time. The least significant bit is transferred first (see figure 4-1). RDY is inhibited after the most significant bit has been transferred to the CCM. Additional input data characters are similarly transferred to the CCM. After a TERC is received, the buffer terminates as previously indicated.

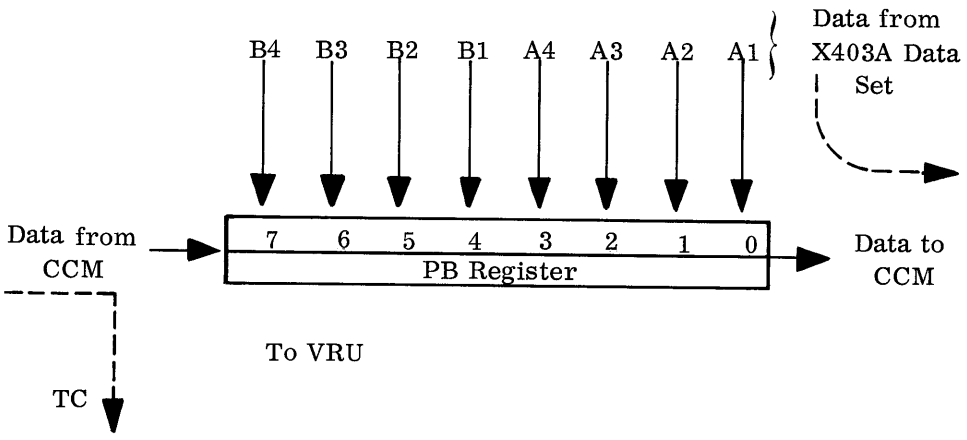


Figure 4-1. Parallel Buffer Data Flow

Transmit (Normal)

◆ The buffer executes a TC and responds to a CCM SEL with RDY. A bit is received from the CCM on the Data lead and shifted into a register. The least significant bit is shifted first (see figure 1). When a complete character (eight bits) is accumulated, RDY is inhibited. At PT the character is shifted, via the Address (A) lead, to the VRU. The shifting is under control of the VRU, which supplies the necessary shift pulses. The least significant bit is shifted first. When WT goes off, the register is reset and RDY is enabled. Thereafter, a character is sent to the VRU every Word Time (WT). After receiving TERC and the last bit, the buffer inhibits RDY and terminates as previously indicated.

Note:

This section applies to operation with a Video Response Unit (VRU).

Transmit (Optional)

◆ The buffer executes a TC and responds to a CCM SEL with RDY. A bit is received from the CCM on the Data lead and shifted into the first state (position 7 in figure 1) of the register, RDY is then inhibited for 10ms. A 1 bit in this position of the register causes Answer Back Control A to be turned on. It remains on as long as 1's are being shifted to the buffer. After receiving TERC and the last bit, the buffer inhibits RDY and terminates as previously indicated.

Note:

This section applies when a Voice Response Unit (VRU) is not employed.

Reports

◆ The Report signals to the CCM are encoded by the buffer to show the following conditions:

Malfunction (MR)	Ring (RR)
Error (ER)	END
End and Error (EER)	Line Disconnect Report (LDR)

Malfunction (MR)

◆ When a Transmit Command (TC) is present and prior to END, the buffer indicates a VRU failure (DOP) to the CCM via a Malfunction Report (MR).

After an MR, the buffer drops the command which was present as it does for a Termination (TERC) as previously indicated and is conditioned to accept a new command.

Line Disconnect Report (LDR)

◆ When a TC or an RC is present, and prior to END, the buffer indicates a disconnect condition to the CCM via an LDR. An LDR is caused by loss of DSR during RC or absence or loss during TC.

If disconnect and malfunction conditions occur simultaneously only the MR is indicated to the CCM.

Ring (RR)

◆ The buffer is conditioned to detect and RI signal from the data set after a DISC. While in the quiescent state, the buffer reports Ring once per RI signal from the data set.

END

◆ The buffer reports END whenever it completes the operations required by each command as previously indicated.

Error (ER)

◆ When a TC is present and prior to END, the buffer indicates incorrect data transfer to the VRU via an ER to the CCM. An ER is caused by presence of data in the buffer at the end of the WT pulse. If disconnect and error conditions occur simultaneously only ER is indicated to the CCM.

END and Error (EER)

◆ The buffer indicates a concurrent END and Error condition by means of the END and Error Report (EER).

Control and Indicators

◆ The operator controls and indicators for the buffer are located on the CCM Control Panel. They consist of the following:

Data (white indicator)- This indicator lights whenever the buffer is exchanging data signals with a remote device.

Select (patch panel) - The buffer is connected to any CCM Select (SEL) line, and is thereby enabled if power is on. When the buffer is enabled, it responds to each SEL with BOP.

Options

◆ The options are field installable and accomplished by simple wiring changes and/or addition of a plug-in.

Non-VRU Operation - This option enables the buffer to modulate the Answer Back Control A lead by using the TC as previously indicated. The VRU cable is not supplied, and the DOP signal is strapped on.

Non-Phrase Operation - If the vocabulary in the VRU contains words only and are repeated three times, then the buffer starts address transfer to the VRU at the first Word Time (WT). If, however, the vocabulary contains phrases or more than sixty-three words (189 word vocabulary) then the first address transferred to the VRU coincides with Phrase Time (PT).

ASYNCHRONOUS DATA SET (ADS) BUFFER, MODEL 70/720

GENERAL DESCRIPTION

◆ The RCA Model 70/720 Asynchronous Data Set Buffer (ADS) occupies one scan position on the Communication Controller-Multichannel (CCM), Model 70/668; and enables it to exchange control and bit-serial data signals with EIA Standard asynchronous data sets (i.e., those which do not provide a data clock pulse) or equivalent. Operation is half-duplex and asynchronous (using START and STOP signal framing elements). In all cases, signal element or bit timing is provided by the buffer for operation at data speeds up to 1800 bits per second. All transmitted signal elements are of integral value. Two buffers and a feature are required for full-duplex operation. Optional capability is provided for using the fast turnaround provided by four-wire, half-duplex circuits.

Reverse-channel signalling and break signal detection are permitted via two and four-wire circuits. A special feature permits automatic calling.

Three models are provided as follows:

Model	Services
70/720-11	TWX (Teletypewriter Exchange-4 row) with interface to CPT (Customer-Provided Terminals).
70/720-21	Message network and private line services with data sets or equivalents.
70/720-22	Same as above except with reverse-channel capability.
70/720-23	Used with IBM 2741 Terminals on private line services.

COMMUNICATION EQUIPMENT AND FACILITIES

◆ The buffer is compatible with the common-carrier communication equipment and facilities indicated below or their equivalents.

Service	Grade	AT&T Data Set	Max. BPS	Buffer Model	Notes
Private Line	Sub-Voice	108/109	150	-21, -22	(4)
Private Line	Voice	103F	300	-21, -22, -23	(1)
Private Line	Voice	202D	1800	-21, -22	(1) (3)
TWX	Sub-Voice	811B	110	-11	(2) (4)
Message Network	Voice	103A	200	-21	(2)
Message Network	Voice	202C	1200	-21, -22	(2) (3)

COMMUNICATION EQUIPMENT AND FACILITIES *(Cont'd)*

Notes:

1. Four-wire (or equivalent), half-duplex operation permitted for fast-turnaround or reverse-channel signalling.
2. Automatic calling permitted via the AT&T 801A or 801C Automatic Calling Unit.
3. Reverse-channel signalling permitted on two-wire circuits.
4. Additional termination equipment is provided as a part of the service.

OPERATIONAL CHARACTERISTICS

◆ The 70/720 series of buffers operate as described in the following paragraphs depending upon the buffer model involved, the remote device and interconnecting facilities involved, and the commands it receives from the CCM.

Signals

◆ Control signals and data bits are exchanged between the buffer and CCM in a prescribed sequence:

1. CCM selects the buffer.
2. The buffer presents its status signals and data level.
3. CCM issues command signals or a data level.
4. CCM drops Select, allowing the buffer to change its status signals and data level.

Signal and data levels are accepted by the buffer and CCM at strobe time. The buffer drops the report levels after receipt of RAK from the CCM.

Commands

◆ The command signals from the CCM are decoded by the buffer into the following commands:

Disconnect (DISC)	Receive (RC)
Transmit (TC)	Auto-Call (ACC)
*End Character (ECC)	Terminate (TERC)

Disconnect (DISC)

◆ The DISC command restores the buffer and the data set to their quiescent conditions; such that a message network line is disconnected at the end of a call.

Transmit (TC)

◆ The TC command conditions the buffer, the data set, and the line for data transmission.

Receive (RC)

◆ The RC command conditions the buffer, the data set, and the line for data reception.

*Model 70/720-11, only.

Terminate (TERC)

◆ The TERC command conditions the buffer to terminate a Transmit, Receive, or Auto-Call command.

End Character (ECC) - Model 70/720-11, Only

◆ The ECC command indicates to the buffer when the last bit of a character has been transmitted.

Data Transfer

◆ Normally the buffer transfers data from the CCM to the data set, and vice versa, with the sense (1 or 0) unchanged; as indicated in subsequent sections.

Initial Conditions

◆ Whenever the buffer receives a SEL from the CCM, it responds with BOP regardless of command status or line condition. In the absence of a command, the buffer remains in the condition in which it is placed upon termination of the previous command. It is then conditioned to receive a new command.

Whenever a signal appears on the Reset lead from the CCM, the buffer is restored to its quiescent condition and the command which was present, if any, is dropped. The buffer responds to subsequent SEL's with BOP only until another command is received.

Transmit

General - All Models

◆ The buffer executes a TC as indicated. Upon receipt of CTS (and optionally, either RD or SRD) from the data set; the buffer responds to a CCM SEL with RDY. A bit is received from the CCM on the Data lead. It is transferred to bit storage and then to the data set TD lead with the same sense (1 or 0) as received from the CCM. Thereafter, the buffer becomes RDY and transfers the second bit to storage. By means of bit timing which the buffer derives from a CCM oscillator, the second bit is transferred to the TD lead at the proper time. Subsequently, bits are transferred to storage and then to the TD lead until TERC is received along with the last bit to be transmitted. Thereafter, the buffer inhibits RDY, transfers the last bit to the TD lead, and terminates as indicated. The buffer places a marking (1) bit on the line unless a spacing (0) bit is made available by the CCM. The buffer does not become RDY when CTS is off.

TWX - Model 70/720-11

◆ In addition to the functions described in the preceding section, TWX operation accommodates the restraint function imposed by the TWX interface. Thus, during TWX transmission, the buffer monitors the RDT signal. When RDT goes on, the buffer stops transmission by inhibiting RDY to the CCM after receiving an ECC from the CCM. The buffer resumes transmission when RDT goes off. If the buffer detects RC spacing for Xms it reports space detected, inhibits RDY, and transmits the bits already received from the CCM. When RD returns to marking transmission is resumed.

Receive

◆ The buffer executes an RC as indicated, and is conditioned to detect a spacing (mark-to-space transition) condition on the data set RD lead when DCD is present. After detecting a spacing condition, by means of bit timing which the buffer derives from a CCM oscillator; a bit is transferred from the RD lead to storage. The buffer then responds to a CCM SEL with RDY. The bit is transferred to the CCM on the Data lead with the same sense (1 or 0) as received from the data set. Subsequently, bits are transferred from the RD lead to storage and then to the CCM until TERC is received. Thereafter, the buffer inhibits RDY and terminates as indicated. Bit timing is restarted on each mark-to-space transition.

Reports

◆ The Report signals to the CCM are encoded by the buffer to show the following conditions:

Report	Bit Configuration		
	REP3	REP2	REP1
Quiescent	0	0	0
END	0	0	1
Error (ER)	0	1	0
End and Error (EER)	0	1	1
Malfunction (MR)	1	0	0
Ring (RR)	1	0	1
Break Detected (BDR)	1	1	0

Malfunction (MR) - All Models

◆ When a command is present in the buffer but after an RDY (except during automatic calling) and prior to END, the buffer indicates improper communication equipment and line conditions to the CCM via a Malfunction Report (MR). An MR is caused by the following:

1. *Transmit* - Loss of the DSR signal from the data set.
2. *Receive* - Loss of the DSR signal from the data set.
*3. *Auto-Call* - A signal from the Auto-Call special feature.

After an MR, upon receipt of RAK from the CCM, the buffer terminates the command and does not report END to the CCM. The buffer is then in the quiescent condition.

*The Auto-Call signal does not apply to the 70/720-23 Buffer, or to the 70/720-21 and 22 Buffers when used with private line applications.

Error (ER) - All Models

◆ When a command is present in the buffer but after an RDY (except where noted or during automatic calling) and prior to END, the buffer indicates an error condition to the CCM via an Error Report (ER). An ER is caused by the following:

1. *Transmit* - Loss of the data set CTS signal, prior to END.
2. *Receive* - Loss of the data set DCD signal, prior to receipt of TERC.
*3. *Auto-Call* - A signal from the Auto-Call special feature.

The buffer reports such conditions once per occurrence.

If error and malfunction conditions occur simultaneously, only the MR is indicated to the CCM.

Ring (RR) - 70/720-11,21,22

◆ The buffer is always conditioned to detect an RI signal from the data set and report a Ring (RR) to the CCM. The buffer reports a Ring only once per RI signal from the data set. The Ring Report, as well as the RI signal from the data set, do not apply to the 70/720-23 Buffer, or to the 70/720-21 and 22 Buffers when used with private line applications.

END - All Models

◆ The buffer reports END whenever it completes the operations required by each command as previously indicated. END is enabled by a TERC or a DISC from the CCM.

END and Error (EER) - All Models

◆ The buffer indicates a concurrent END and error condition by means of the END and Error Report (EER). When using the 70/720-23 Buffer, EER is caused by the sensing of 14 ms. of spacing on the RD lead from the data set.

Break Detected (BDR)

◆ When a TC is present in the Buffer, but after an RDY and prior to END, the buffer indicates a reverse channel signal detected to the CCM via BDR. BDR is caused by the following:

Model 70/720-11 - upon detecting RD spacing continuously for X ms.

Model 70/720-21 - not applicable to this buffer.

Model 70/720-22 - upon detecting:

1. RD spacing continuously for X ms; or optionally
2. SRD OFF for X ms; or optionally
3. Reverse channel implementation option
4. X is normally set to 50 ms but may be set to any point in the range of :20-115 ms.

Model 70/720-23 - upon detecting RD spacing continuously for 140 ms.

*The Auto-Call signal does not apply to the 70/720-23 Buffer, or to the 70/720-21 and 22 Buffers when used with private line applications.

Communications Interface

◆ The buffer operates with a communications interface (to data sets, automatic calling units, etc.) which conforms to EIA Standard RS-232-B (interface between data processing terminal equipment and data communication equipment).

The buffer can be operated without data sets when provision for such operation is made in the appropriate remote device or system.

Controls and Indicators

◆ The operator controls and indicators for the buffer are located on the CCM Control Panel. They consist of the following:

Data (amber indicator) - With a TC present, this indicator lights except when a spacing bit is transmitted. With an RC present, after the first mark-to-space transition, this indicator lights except when a spacing bit is received.

Select (patch panel) - The buffer is easily connected to any CCM Select (SEL) line and is thereby enabled when power in ON. When the buffer is enabled, it responds to each SEL with BOP.

Options

◆ The buffer options described below are field-installable via wiring changes. The buffer is originally conditioned for half-duplex, two-wire operation, without any of the options.

Buffer Options

◆ *Four-Wire Operation* - This option is employed to eliminate the data set turnaround delay with certain communications services and data sets as follows:

Service	AT&T Data Set
Dialed Network (2-wire)	103A
Half and Full Duplex	103F
Half and Full Duplex	202D

The effect of the option is as follows:

The RS signal to the data set is strapped in the on condition. Thus, whenever CTS is on, transmission can begin.

1. This option applies only to the Model 70/720-21

2. This option can only be used when there is sufficient receive-to-transmit turnaround delay built into the devices at each end of the communications channel to allow each to accomplish the turnaround from transmit-to-receive.

Buffer Options (Cont'd)

Reverse Channel Signal Detection Model 70/720-22 - This function effective during transmission for break signal detection with some teletypewriter systems and for detection of reverse channel error and channel assurance signals. The operation of this function is as follows:

After receipt of a TC, transmission cannot start until RD is marking (or, optionally, SRD is on) continuously for X ms. While transmitting, a break detected is reported if RD goes spacing (or, optionally, SRD is off) continuously for X ms. The buffer then inhibits RDY while RD is spacing, but transmits the bits already received from the CCM. When RD returns to the marking condition, transmission is resumed.

The X ms duration of the reverse signal is adjustable. It is normally set to 50 ms, but it may be set to any point in the range of 20 to 115 ms.

Reverse Channel Signal Generation - Model 70/720-22, Only - This function is effective during reception for generation of reverse channel error and channel assurance signals. The effect of the option is as follows:

After receipt of an RC, the buffer turns STD on. Upon termination (TERC) of an RC, the buffer turns STD off (or, optionally, TD spacing) for Y ms, then it responds to a SEL with END and returns TD marking.

1. Y is normally set to 200 ms, but may be set to any point in the range: 115-750 ms.
2. This causes END to be delayed for Y ms after TERC for both the TC and the ACC as well as the RC.

Data Gathering System (DGS) - Model 70/720-22, Only - This option enables the buffer and associated data set (AT&T 202D or equivalent) to communicate with a Data Gathering System Input Station via a Line Concentrator. The effect of this option is as follows:

DTR is strapped on. RS is strapped on. After receipt of an RC, the buffer turns TD on. TD is on until RC is terminated whereupon it is turned off. This option may only be used with four-wire private line facilities.

Communication Equipment Options

◆ At installation, the data set must be conditioned (by the common carrier upon request) as follows:

AT&T 103A Data Set - Automatic Answer - controlled by AUTO key.
Initiate Disconnect - Yes.
Respond to Disconnect - No.

AT&T 103F Data Set - Mode-local: Originate, remotes: Answer; at all times.

AT&T 202C Data Set - Automatic Answering - controlled by AUTO key.

AT&T 202D Data Set - Two or four-wire operation.

FEATURE 5705 - AUTO-CALL FEATURE

◆ This feature, together with an AT&T 801A or 801C Automatic Calling Unit (or equivalent) enables one buffer to dial automatically and connect a communication line under control of the processor and CCM. The Automatic Calling Unit (ACU) and this special feature can only be used with a data set which operates on the message network, or with TWX.

This special feature can be installed in the factory or in the field.

OPERATIONAL CHARACTERISTICS

Auto-Call Command (ACC)

◆ This command is used only for a buffer equipped with the Auto-Call feature. The function of an ACC is to condition the buffer and feature, as well as the Automatic Calling Unit, for transfer of dialing digits.

When the buffer decodes an Auto-Call Command (ACC), it so notifies this feature which turns CRQ on. Upon termination (TERC) of the ACC, this feature is notified. Thereafter, when DSS or DSR comes on, this feature turns CRQ off and notifies the buffer to respond to a SEL with END.

When employed with the 70/720-22 buffer, END is delayed after DSR comes on.

Digit Transfer

◆ The buffer executes an ACC as indicated. When PND is received from the ACU, this feature causes the buffer to respond with RDY on four successive SELs. When the four bits which represents the digit to be dialed are received from the CCM, they are made available to the ACU on the digit Leads by turning DPR on. DPR remains on until the ACU drops PND. When PND comes on, this feature causes the buffer to become RDY as before. This process continues until TERC along with the last bit of the last digit to be dialed is received from the CCM. Thereafter, this feature causes the buffer to terminate as indicated in the previous section.

Reports

Malfunction (MR)

◆ Upon notification that an ACC is present in the buffer, this feature notifies the buffer whenever PWI goes off. The buffer, in turn, immediately issues an MR to the CCM.

Error (ER)

◆ Upon notification that an ACC is present in the buffer, this feature notifies the buffer during the next CCM SEL if the ACU DLO lead is on. Thereafter, the DLO lead is not monitored by this feature. The buffer immediately reports the Error to the CCM and turns CRQ off.

END and Error (EER)

◆ When an ACC is present, this feature notifies the buffer whenever the ACR lead from the ACU is on. The buffer generates an END and Error Report to the CCM and turns CRQ off.

Options

Automatic Calling Unit Options

◆ The AT&T 801 Automatic Calling Unit must be conditioned by the common-carrier at installation with the indicated options described in the appropriate Bell System Technical Reference. The ACU options used with this buffer are:

Option Y - ACR timer stops in DATA mode.

Option Z - Call termination via data set.

FEATURE 5714 - FULL-DUPLEX OPERATION

◆ This feature enables a pair of buffers (Model 70/720-21, only) to be used for full-duplex operation on leased lines with any of the following data sets (or equivalents): AT&T 103F and 202D. One of the buffers is always the transmitter and the other is always the receiver. This feature precludes the Auto-Call feature and the buffer option. It can be installed in the factory or in the field.

COMMANDS AND DATA TRANSFER

◆ This special feature does not affect the buffer command and data transfer functions. However, the program must route the proper commands to the associated pair of buffers.

REPORTS

◆ The report functions of the individual buffers apply when this feature is implemented, except that there will be no ring reports.

OPTIONS

◆ None. However, the communications facilities and data sets must be conditioned for full-duplex operation.

SYNCHRONOUS DATA SET (SDS) BUFFER, MODEL 70/721

GENERAL DESCRIPTION

◆ The RCA Model 70/721 Synchronous Data Set Buffer (SDSB) occupies one scan position on the Communications Controller-Multichannel (CCM), Model 70/668; and enables it to exchange control and bit-serial data signals with EIA-Standard synchronous data sets (i.e., those which provide a data clock pulse). Operation is half-duplex, synchronous, at speeds of 2000 or 2400 bits per second. Two buffers and a special feature are required for full-duplex operation. Optional capability is provided for using the fast-turnaround provided by four-wire half-duplex circuits. A feature permits automatic calling.

COMMUNICATION EQUIPMENT AND FACILITIES

◆ The buffer is compatible with the common-carrier communication equipment and facilities indicated below or their equivalents.

Service	Grade	AT&T Data Set	Data Capacity	Notes
Private Line	Voice	201B	2400 bps	(1)
Message Network	Voice	201A3	2000 bps	(2)

Notes:

1. Four-wire, half-duplex operation permitted for fast-turnaround.
2. Automatic calling permitted via the AT&T 801A or 801C Automatic Calling Units.

OPERATIONAL CHARACTERISTICS

◆ Control signals and data bits are exchanged between the SDSB and CCM in a prescribed sequence:

1. The CCM selects the buffer;
2. The buffer presents its status signals and data level;
3. The CCM issues command signals and a data level; and
4. The CCM drops Select, allowing the buffer to change its status signals and data level.

Note:

Signal and data levels are accepted by the buffer and CCM at strobe time. The buffer drops the reports levels after receipt of RAK from the CCM.

Commands

◆ The command signals from the CCM are decoded by the buffer into the following commands:

Disconnect (DISC)

◆ The DISC command restores the buffer and the data set to their quiescent conditions such that a message network line is disconnected at the end of a call.

Transmit (TC)

◆ The TC command conditions the buffer, the data set, and the line for data transmission.

Auto-Call (ACC)

◆ The ACC command is used only for a buffer equipped with the Auto-Call Special Feature. The ACC command conditions the buffer and special feature, as well as the Automatic Calling Unit, for transfer of dialing digits.

Receive (RC)

◆ The RC command conditions the buffer, the data set, and the line for data reception.

Terminate (TERC)

◆ The TERC command conditions the buffer to terminate a Transmit, Receive, or Auto-Call command.

Data Transfer

◆ The buffer transfers data from the CCM to the data set, and vice versa, with the sense (1 or 0) unchanged as indicated in subsequent sections of this manual.

Initial Conditions

◆ Whenever the buffer receives a SEL from the CCM, it responds with BOP regardless of command status or line condition. In the absence of a command, the buffer remains in the condition in which it is placed upon termination of the previous command. It is then conditioned to receive a new command.

Whenever a signal appears on the Reset lead from the CCM, the buffer is restored to its quiescent condition and the command which was present, if any, is dropped. The buffer responds to subsequent SELs with BOP only until another command is received.

Transmit

◆ The buffer executes a TC as indicated. Upon receipt of CTS from the data set, the buffer responds to a CCM SEL with RDY. A bit is received from the CCM on the Data lead and transferred to bit storage. By means of bit timing which the buffer receives on the data set SCT lead, the bit is transferred to the data set TD lead with the same sense (1 or 0) as received from the CCM. Thereafter, the buffer becomes RDY and transfers the second bit to storage. Using data set timing, the second bit is transferred to the TD lead at the proper time. Subsequently, bits are transferred to storage and then to the TD lead until TERC is received along with the last bit to be transmitted. Thereafter, the buffer inhibits RDY, transfers the last bit to the TD lead, and terminates the command.

Notes:

1. The buffer places a marking (1) bit on the line unless a spacing (0) bit is made available by the CCM.
2. The buffer does not become RDY when CTS is off.

Receive

◆ The buffer executes an RC as indicated, and is conditioned to start bit detection when DCD is present. By means of bit timing which the buffer receives on the data set SCR lead; a bit is transferred from the data set RD lead to storage. The buffer then responds to a CCM SEL with RDY. The bit is transferred to the CCM on the Data lead with the same sense (1 or 0) as received from the data set. Subsequently, bits are transferred from the RD lead to storage and then to the CCM until TERC is received. Thereafter, the buffer inhibits RDY and terminates as indicated.

Reports

◆ The Report signals to the CCM are encoded by the buffer to show the following conditions:

Malfunction (MR)	Ring (RR)
Error (ER)	END
END and Error (EER)	

Malfunction (MR)

◆ When a command is present in the buffer, but after an RDY (except during automatic calling) and prior to END; the buffer indicates improper communication equipment and line conditions to the CCM via a Malfunction Report (MR). An MR is caused by the following:

1. *Transmit* - Loss of the DSR signal from the data set.
2. *Receive* - Loss of the DSR from the data set.
3. *Auto-Call* - A signal from the special feature.

After an MR, upon receipt of RAK from the CCM, the buffer terminates the command and does not report END to the CCM. The buffer is then in the quiescent condition.

Error (ER)

◆ When a command is present in the buffer, but after an RDY (except where noted or during automatic calling) and prior to END; the buffer indicates an error condition to the CCM via an Error Report (ER). An ER is caused by the following:

1. *Transmit* - Loss of the data set CTS signal, prior to receipt of TERC.
2. *Receive* - Loss of the data set DCD signal, prior to receipt of TERC.
3. *Auto-Call* - A signal from the special feature.

The buffer reports such conditions once per occurrence.

If error and malfunction conditions occur simultaneously, only the MR is indicated to the CCM.

Ring (RR)

◆ The buffer is always conditioned to detect an RI signal from the data set and report a Ring (RR) to the CCM. The buffer reports a Ring only once per RI signal from the data set.

END

◆ The buffer reports END whenever it completes the operations required by each command as previously indicated. END is enabled by a TERC or a DISC from the CCM.

End and Error (EER)

◆ The buffer indicates a concurrent END and error condition by means of the END and Error Report (EER).

Communications Interface

◆ The buffer shall operate with a communications interface (to data sets, automatic calling units, etc.) which conforms to EIA Standard RS-232-B - Interface between Data Processing Terminal Equipment (DPTE) and Data Communication Equipment (DCE). The buffer cannot be operated without an appropriate data set or equivalent EIA interface.

Controls and Indicators

◆ The operator controls and indicators for the buffer are located on the CCM Control Panel. They consist of the following:

Data (amber indicator) - With a TC present, this indicator is illuminated except when a spacing bit is transmitted. With an RC present, this indicator lights except when a spacing bit is received.

Select (patch panel) - The buffer is easily connected to any CCM Select (SEL) line, and is thereby enabled when power is on. When the buffer is enabled, it responds to an SEL with BOP.

Options

◆ The buffer options are field-installable via wiring changes. The buffer is originally conditioned for half-duplex, two-wire operation, without any of the options. See buffer special features.

The communications equipment options are installed, upon request, by the common carrier.

Buffer Options

◆ *Four-Wire Operation* - This option is employed to eliminate the AT&T 201B data set turnaround delay when using 4-wire private line for half-duplex data transmission.

The effect of the option is as follows:

The RS signal to the data set is strapped in the ON condition. Thus whenever CTS is ON, transmission can begin.

Private Line Operation - This option must be used with an AT&T 201B data set or equivalent (for private line operation). The effect of this option is as follows: Remote Release is strapped to Remote Control (DTR ON) and Ready is strapped to Remote Release. When this option is installed the Disconnect Command cannot be used and Ring Reports are not generated.

Data Terminal Ready (DTR) - When this option is installed the buffer turns DTR off when a Transmit or Receive Command is terminated.

Communication Equipment Options

◆ At installation, the data set must be conditioned as follows:

AT&T 201A3 Data Set - Automatic Answer - controlled by AUTO key.

AT&T 201B Data Set -New Sync (NS) - strap out if not required (normal). The NS option is used for two or four-wire multi-station lines.

FEATURE 5705 - AUTO-CALL FEATURE

◆ This feature together with an AT&T 801A or 801C Automatic Calling Unit (or equivalent) enables one buffer to dial automatically and connect a communication line under control of the processor and CCM. The Automatic Calling Unit (ACU) and this special feature can only be used with a data set which operates on the message network.

This special feature can be installed in the factory or in the field.

OPERATIONAL CHARACTERISTICS

Auto-Call Command (ACC)

◆ This command is used only for a buffer equipped with the Auto-Call feature. The function of an ACC is to condition the buffer and feature, as well as the Automatic Calling Unit, for transfer of dialing digits.

When the buffer decodes an Auto-Call Command (ACC), it so notifies this feature which turns CRQ on. Upon termination (TERC) of the ACC, this feature is notified. Thereafter, when DSS comes on, this feature turns CRQ off and notifies the buffer to respond to a SEL with END.

Digit Transfer

◆ The buffer executes an ACC as indicated. When PND is received from the ACU, this feature causes the buffer to respond with RDY on four successive SELs. When the four bits which represents the digit to be dialed are received from the CCM, they are made available to the ACU on the digit Leads by turning DPR on. DPR remains on until the ACU drops PND. When PND comes on, this feature causes the buffer to become RDY as before. This process continues until TERC along with the last bit of the last digit to be dialed is received from the CCM. Thereafter, this feature causes the buffer to terminate as indicated in the previous section.

Reports

Malfunction (MR)

◆ Upon notification that an ACC is present in the buffer, this feature notifies the buffer whenever PWI goes off. The buffer, in turn, immediately issues an MR to the CCM.

Error (ER)

◆ Upon notification that an ACC is present in the buffer, this feature notifies the buffer, during the next CCM SEL if the ACU DLO lead is on. Thereafter, the DLO lead is not monitored by this feature. This feature also notifies the buffer whenever the ACU ACR lead is on. When the ACR lead is on, the buffer reports END and ERROR to the CCM, and turns CRQ off.

Automatic Calling Unit Options

◆ The AT&T 801A Automatic Calling Unit must be conditioned by the common-carrier at installation with the indicated options described in Bell Technical Reference: Data Auxiliary Set 801A (Automatic Calling Unit) Interface Specification.

Y - ACR timer stops in DATA mode.

Z - Call termination via data set.

FEATURE 5714 - FULL-DUPLEX OPERATION

◆ This feature enables a pair of buffers to be used for full-duplex operation on leased lines with the following data set (or equivalent): AT&T 201B1. One of the buffers is always the Transmitter and the other is always the Receiver. This feature precludes the Auto-Call Feature and the Four-Wire Operation option. It can be installed in the factory or in the field.

OPERATIONAL CHARACTERISTICS

Signals

◆ Refer to the buffer descriptions and their operation with data sets for definition of the signals exchanged between the applicable buffer and data set.

Commands and Data Transfer

◆ This feature does not affect the buffer command and data transfer functions. However, the program must route the proper commands to the associated pair of buffers.

Reports

◆ The report functions of the individual buffers are as previously described except that there will be no Ring Reports.

Options

◆ None. However, the communications facilities and data sets must be conditioned for full-duplex operation.

SYNCHRONOUS TRANSMITTER-RECEIVER BUFFER (STRB), MODEL 70/722

GENERAL DESCRIPTION

◆ The STRB occupies one scan position on the Communication Controller-Multichannel (CCM), Model 70/668; and enables it to exchange control and bit-serial data signals with another STRB or with IBM Synchronous Transmitter-Receiver terminals, via EIA-Standard data sets. The character length is fixed at eight bits. Operation is always half-duplex and synchronous, with signal element or bit timing supplied to the data set by the STRB. Such timing is derived from oscillators in the CCM and permits data speeds up to 2400 bits per second. Optional capability is provided for using the fast-turnaround provided by four-wire, half-duplex circuits.

OPERATIONAL CHARACTERISTICS

STRB/CCM Interface

◆ Control signals and data bits are exchanged between the STRB and CCM in a prescribed sequence:

1. The CCM Selects the STRB,
2. The STRB presents its status signals and data level,
3. The CCM issues command signals and a data level, and
4. The CCM drops Select, allowing the STRB to change its status signals and data levels.

Note:

Signal and data levels are accepted by the STRB and CCM at Strobe time.

Commands

◆ The command signals from the CCM are decoded by the STRB into the following commands:

Disconnect (DISC)	Receive (RC)
Transmit (TC)	Terminate (TERC)

End Character (ECC)

Disconnect (DISC)

◆ The DISC command restores the STRB and the data set to their quiescent conditions such that a message network line is disconnected at the end of a call and carrier is dropped on a private line.

Transmit (TC)

◆ The TC command conditions the STRB, the data set, and the line for data transmission.

Receive (RC)

◆ The RC command conditions the STRB, the data set, and the line for data reception.

Terminate (TERC)

◆ The TERC command conditions the buffer to terminate a Transmit, Receive, or Auto-Call command.

End Character (ECC)

◆ The ECC command sets the STRB character frame for receiving. The STRB does not respond with END.

Data Transfer

Initial Conditions

◆ Whenever the STRB receives a SEL from the CCM, it responds with BOP regardless of command status or line condition. In the absence of a command, the STRB remains in the condition in which it is placed upon termination (END) of the previous command. It is then conditioned to receive a new command.

Whenever a signal appears on the Reset lead from the CCM, the STRB is restored to its quiescent condition and the command which was present, if any, is dropped. The STRB responds to a subsequent SEL with BOP, only; until another command is received.

Synchronization

◆ The STRB provides both character and bit synchronization with the remote transmitter-receiver. While transmitting, the STRB employs a fixed-character frame to which the remote receiver synchronizes. While receiving, the STRB relies on the CCMs character recognition capability to establish the character frame. Once the CCM sets the frame via the ECC, the STRB retains that frame until a new frame is set by the CCM. While receiving, the STRBs bit detection point is initially fixed; and then corrected (advanced or retarded) in accord with the received signal transitions. Each correction amounts to 3% of a bit time. This process is described in detail in the appropriate IBM literature. The method of achieving synchronous is as follows:

1. *Transmit* - If the STRB is to transmit, the program must first enable synchronization by the remote receiver and receives an End of Idle (EOI). To initiate this process, the program transmits a minimum of 100 Idle characters, followed by an EOI. The program then places the CCM and STRB in the receive mode and awaits receipt of an End of Idle (EOI) Sequence. If EOI is not received in 3 seconds (program timing), the program resumes transmission of Idles followed by EOI; and again goes to receive. When an EOI has been received, the program can request permission to transmit by sending an Inquiry.

2. *Receive* - If the STRB is to receive, the program must first enable synchronization of the STRB. To initiate this process, the program places the CCM and STRB in the receive mode and awaits receipt of an End of Idle (EOI) or an Inquiry. If an EOI is received, the program transmits a minimum of 100 Idle characters, followed by an EOI, and again goes to receive. If an inquiry is received, the program transmits the response.

Data Transmission

◆ The STRB executes a TC as indicated. When DSR and DCD from the data set are present, the STRB responds to a CCM SEL with RDY. A bit is received from the CCM on the Data lead and transferred to bit storage. At the proper time, the STRB's transmit clock causes the stored bit to be transferred to the data set TD lead with the same sense (1 or 0) as received from the CCM. Thereafter, so long as DSR and CTS are present, the STRB becomes RDY and transfers the second and subsequent bits to storage and then to the TD lead until TERC is received along with the last bit to be transmitted. After receiving TERC, the STRB inhibits RDY, transfers the last bit to the TD lead, and terminates as indicated.

While a TC is present, the STRB places a marking (1) bit on the TD lead unless a spacing (0) bit is made available by the CCM.

Data Reception

◆ The STRB executes an RC as indicated. When DSR and DCD from the data set are present, the STRB is conditioned to transfer the first bit from the RD lead to bit storage, using the character frame previously established. The STRB then responds to a CCM SEL with RDY. The stored bit is transferred to the CCM on the Data lead with the same sense (1 or 0) as received from the RD lead. Subsequently, so long as DSR and DCD are present, bits are transferred from the RD lead to bit storage and then to the CCM. If at any time the buffer receives an ECC from the CCM, it adjusts the character frame so that the next bit is the first of a sequence of eight bits in the frame. After a TERC is received, the STRB inhibits RDY and terminates as indicated.

Upon entering the receive mode with DSR and DCD present, the STRB does not transfer a bit to storage until the first bit of the character frame comes up.

Timing

◆ The STRB provides the bit or signal element timing for operation with all data sets. This timing is derived from the modulation rate oscillators in the CCM.

Reports

◆ The Report signals to the CCM are encoded by the STRB to show the following conditions:

Malfunction (MR)	Ring (RR)
Error (ER)	END

END and Error (EER)

Malfunction (MR)

◆ When a command is present, but after a RDY and prior to END; the STRB indicates improper communication equipment and line conditions to the CCM via a Malfunction Report (MR). An MR is caused by the following:

1. Transmit - Loss of the CTS signal from the data set, prior to TERC.
   - Loss of the DSR signal from the data set.
2. Receive - Loss of the DSR signal from the data set.

After an MR, the STRB drops the command which was present as it does for a termination (TERC) as previously indicated and is conditioned to accept a new command.

Error (ER)

◆ When a command is present, but after an RDY (except during automatic calling) and prior to END; the STRB indicates an error condition to the CCM via an Error Report (ER). An ER is caused by the following:

1. Transmit - None.

2. Receive - Loss of the data set DCD signal, prior to TERC.

The STRB reports such conditions once per occurrence.

If error and malfunction conditions occur simultaneously, only the MR is indicated to the CCM.

Ring (RR)

◆ The STRB is always conditioned to detect an RI signal from the data set and report a Ring (RR) to the CCM; except when a Disconnect or a Receive command is present (i.e., prior to END).

The STRB reports a Ring only once per RI signal from the data set.

END

◆ The STRB reports END whenever it completes the operations required by each command as previously indicated. END is enabled by a TERC or a DISC from the CCM.

END and Error (EER)

◆ The STRB indicates a concurrent END, and error condition by means of the END and Error Report (EER).

Controls and Indicators

◆ The operator's controls and indicators for the STRB are located on the CCM Control Panel. They consist of the following:

1. *Data (white indicator)* - This indicator lights whenever the STRB exchanges data signals with a remote device.

2. *Select (patch panel)* - The STRB is easily connected to any CCM Select (SEL) line, and is thereby enabled if power is on. When the STRB is enabled, it responds to each SEL with BOP.

Options

◆ The STRB options covered are field-installable via wiring changes, depending upon the requirements of the remote device and communication facility. These options affect the STRB line control functions upon initiation and termination of Transmit and Receive Commands. The STRB is originally conditioned for half-duplex, two-wire operation.

STRB Options

◆ *Half-duplex, Two-Wire* - This mode of operation is employed when operating half-duplex, two-wire. The effect of the option is as follows:

1. *Transmit* - Upon initiation, RS and DTR are turned on; and RDY is enabled with DSR and CTS are on. Upon termination, one MS after the last bit is transmitted, RS is turned off and END occurs.

2. *Receive* - Upon initiation, DTR is turned on; and RDY is permitted when DSR and DCD are on.

STRB Options (Cont'd)

**Half-Duplex, Four-Wire* - This mode of operation is employed for fast-turnaround when operating half-duplex, four-wire. The effect of the option is as follows:

1. *Transmit* - Upon initiation,RS and DTR are turned on; and RDY is enabled when DSR and CTS are on. Upon termination, RS remains on; and END occurs after the last bit is transmitted.

2. *Receive* - Upon initiation, RS and DTR are turned on; and RDY is permitted when DSR and DCD are on. Upon termination, END occurs immediately.

Speed Selection - At installation, the STRB must be connected to the proper modulation rate oscillator in the CCM.

Communication Equipment Options

◆ The communication equipment options upon request, by the common-carrier.

At installation, the data set must be conditioned as follows:

1. *AT&T 201A3 or 202C* - Automatic answering - controlled by AUTO key.

2. *AT&T 201B or 202D* - Condition for two-wire or four-wire (simultaneous) operation.

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*This option can only be used when the remote transmitter-receiver provides sufficient turnaround delay to allow for command termination and initiation by the CCM and program. Typically, IBM STR equipment does not provide sufficient delay.

EDGE DEMODULATOR/ BUFFER (EDB), MODEL 70/724

GENERAL DESCRIPTION

◆ The RCA Model 70/724 EDGE Demodulator/Buffer (EDB) occupies one scan position of the Communication Controller-Multichannel (CCM), Model 70/668, and enables the CCM to service one output trunk of an EDGE Line Concentrator (LC), Model 6235-3. Buffer operation is asynchronous at a modulation rate of 250 bits per second (27.7 characters per second). This modulation rate is obtained through the use of a 4KC oscillator. Except for returning the Message Acknowledged (ACKC), and control signals to the remote device, the Edge Demodulator/Buffer, a one-way, receive only buffer.

COMMUNICATION EQUIPMENT AND FACILITIES

◆ The Edge Demodulator/Buffer operates with basic two-wire, telephone circuits, which can be either privately owned and installed or leased from a common carrier. The Edge Demodulator/Buffer can be connected to four-wire facilities leased from a common carrier provided these facilities meet certain requirements. Such four-wire facilities and common carrier data sets are required only when the Long Line Option is used for applications where the buffer and its serving Line Concentrator are physically separated by a considerable distance. The Edge Demodulator/Buffer contains its own modem or data set which is comparable to the modem provided with each EDGE Input Station (IS), Model 6220-3.

OPERATIONAL CHARACTERISTICS

◆ Control signals and data bits are exchanged between the buffer and CCM in a prescribed sequence:

1. The CCM selects the buffer.
2. The buffer presents its status signals and data level.
3. The CCM issues command signals.
4. The CCM drops Select, allowing the buffer to change its status signals and data level.

Signal and data levels are accepted by the buffer and CCM at Strobe time.

The EDB/Line Concentrator interface consists of a pair of wires over which ac signals (data, AB1, and AB2) and dc levels (RT and Ready) are exchanged. When the Long Line Option is used, the AC signals and DC levels are transferred on separate circuit pairs.

Commands

◆ The command signals from the CCM are decoded by the Edge Demodulator Buffer into the following commands:

Disconnect (DISC)	Receive (RC)
Acknowledge (ACKC)	Terminate (TERC)

Disconnect (DISC)

◆ The DISC command disables the Line Concentrator trunk thereby preventing the Line Concentrator from connecting an Input Station to that trunk. This is the quiescent condition for the Edge Demodulator/Buffer.

Acknowledge (ACKC)

◆ The ACKC buffer causes the Edge Demodulator/Buffer to respond to a valid message by sending an AB2 to the connected Input Station via the Line Concentrator.

Receive (RC)

◆ The RC command enables the Edge Demodulator/Buffer to accept a message from the Line Concentrator.

Terminate (TERC)

◆ The TERC command terminates a Receive (RC) command.

Data Transfer

Initial Conditions

◆ Whenever the Edge Demodulator/Buffer receives a SEL from the CCM, it responds with BOP regardless of command status or line condition. In the absence of a command, the buffer remains in the condition in which it is placed upon termination (END) of the previous command. It is then conditioned to receive a new command.

Whenever a signal appears on the Reset lead from the CCM, the buffer is restored to its quiescent condition, and the command which was present, is dropped. The buffer responds to subsequent SEL with BOP, until another command is received.

Receive

◆ If an RC is present in the Edge Demodulator/Buffer when the RT signal from the Line Concentrator is sensed, the buffer responds with the AB1 signal which permits the connected Input Station to transmit. The buffer is conditioned to start phase detection after 8 ± 4 ms of unmodulated signal carrier is received. After detecting a phase change, a bit is transferred from the line to bit storage within the buffer.

The Edge Demodulator/Buffer then responds to a CCM SEL with RDY. The bit is transferred to the CCM on the Data lead with the opposite sense as received from the line (1 or 0). Subsequent bits are transferred from the line to storage and then to the CCM until a TERC is received from the CCM. The buffer then inhibits RDY and terminates.

Reports

◆ The Report signals to the CCM are encoded by the Edge Demodulator/Buffer to indicate the following conditions:

ERROR (ER), END

ERROR

◆ The Edge Demodulator/Buffer indicates a loss of signal carrier to the CCM via an ER whenever an RC is present, but after RDY and prior to TERC.

END

◆ The Edge Demodulator/Buffer reports END whenever it completes the operations required by each command.

Message Validation

◆ The EDGE System requires that each message, transmitted from an Input Station, be checked, and that each valid message cause a Message Acknowledged signal (AB2) to be returned to the EDGE Input Station. Three methods of checking are permitted. Any combination may be used in an EDGE System, but only one method can be employed for each Line Concentrator and its associated Edge Demodulator/Buffers. In all cases, the buffer generates the AB2 signal upon receipt of an ACKC from the CCM.

CCM Acknowledgement of all Messages

◆ Each character is checked for correct parity, and upon detection of the End Message (EM) character, the CCM generates ACKC to the Edge Demodulator/Buffer if no error was detected.

Program Validation of all Messages

◆ Each character is checked for correct parity by the CCM, and upon detection of EM, the CCM transfers validation responsibilities to the program. If the message is acceptable, the program generates an Acknowledge Write Control to the CCM, and then to the Edge Demodulator/Buffer. This method of operation requires that the Input Stations which the buffer services be equipped with the Delayed Retransmission Option - Feature 438.

CCM Acknowledgement of Transaction 0 Messages

◆ If the transaction code of a message is 0, indicating an attendance recording, the CCM generates an ACKC immediately upon detection of the EM provided no parity errors have been detected. Program Validation is used for all messages which are not identified as transaction 0 transmissions. This method of operation requires that all Input Stations which the Edge Demodulator/Buffer services be equipped with the Delayed Retransmission Option - Feature 438.

Signal Characteristics

◆ The EDGE System controls data flow via specific ac and dc signals which are initiated at specific times or under certain circumstances.

Transmitted Signals

◆ The following signals are transmitted by the Edge Demodulator/Buffer to the Line Concentrator or to the Input Stations. These three signals comprise the total transmitting capabilities of the buffer.

Ready - DC Signal - The Edge Demodulator/Buffer indicates a ready condition to the Line Concentrator by means of a dc contact closure.

AB1 and AB2 - AC Signals - The Edge Demodulator/Buffer transmits the Permission to Transmit - AB1, and Message Acknowledged - AB2 signals to the Input Stations. These signals are identical and consist of 20 ± 5 ms of unmodulated, signal carrier with a frequency of 2000 cycles.

Received Signals

◆ *Request to Transmit (RT)* - DC Signal - The Edge Demodulator/Buffer recognizes that an Input Station has been connected to it within 21 ms after the Line Concentrator closes the "Request to Transmit" (RT) contact. This contact remains closed as long as the Input Station is connected. 21 ms after the RT contact opens, the buffer recognizes that the Input Station has been disconnected.

Data - AC Signals - The Edge Demodulator/Buffer accepts data in the form of a 2000 cycle carrier signal, modulated at a rate of 250 bits per second.

Controls and Indicators

◆ The operator's controls and indicators for the Edge Demodulator/Buffer are located on the CCM Control Panel.

Data (White indicator) - This indicator is lighted whenever the Edge Demodulator/Buffer is receiving data signals from an EDGE Input Station.

Select (Patch Panel) - The Edge Demodulator/Buffer can be connected to any CCM Select (SEL) line through this device and is enabled when power is on.

Long Life Option

◆ This option permits the Edge Demodulator/Buffer to operate with four-wire common carrier circuits in application requiring the physical separation of the Edge Demodulator/Buffer and its servicing Line Concentrator by considerable distance. This option enables the dc signal circuit to be isolated from the ac signal circuit so that two separate pathways are provided.

Program Considerations

◆ Each EDGE message transferred to the processor memory by the CCM is framed by Start Message (SM) and End Message (EM) characters. In the event an error occurs, the CCM immediately reports it to the program and terminates the command. No further data is transferred to memory until the command is restored and an SM is received from the transmitter.

DATA GATHERING SYSTEM BUFFER (DCS) 70/725

GENERAL DESCRIPTION

◆ The basic buffer unit, Model 70/725, comprises two independent buffers each of which occupies one scan position of the CCM, and enables it to service one output trunk of a DGS Line Concentrator. Operation is synchronous at a speed of 120 characters per second (960 bits per second). Characters are received bit-serially, with character recognition performed by the CCM. This unit is insensitive to code.

COMMUNICATION EQUIPMENT AND FACILITIES

◆ This buffer can be connected directly to AT&T schedule 4, type 4, two-wire data circuits, or equivalent privately-owned facility. This buffer contains a built-in modem.

This unit presents a 600 ohm balanced-line condition for ac signals. The buffer recognizes and produces dc and ac signals which it interchanges with ISs, via an LC.

OPERATIONAL CHARACTERISTICS

◆ All references to the Buffer in this section apply to one of the two functionally independent units comprised by the Model 70/725.

Commands

◆ The command signals (CCM) from the CCM are decoded by this unit into the following commands:

Command	COM3	COM2	COM1
Receive (RC)	0	1	0
Terminate (TERC)	1	0	0
Acknowledge (ACKC)	1	1	1
Not-Acknowledge (NAKC)*	1	1	0
Disable (DIS)**	1	0	1
Transmit	0	0	1

*This COM combination is normally issued by the CCM as Disconnect (DISC). This function is not performed by the DGS Buffer, and the Command is interpreted by this unit as a NAKC.

**This CCM combination is normally issued by the CCM as Auto-Call (ACC). This function is not performed by a DGS Buffer and the Command is interpreted by this unit as a Disable (DIS).

Receive (RC) and Terminate (TERC)

The Receive command enables this unit to accept a message from the line. Upon reception of an RC, the Buffer performs the following functions:

Sets idle current;

Senses RT from the line;

Responds with PT;

Permits carrier and phase detection;

Permits RDY when data is detected; and

Permits reports.

When an RC is terminated (TERC), this unit performs the following functions:

Resets Read Command FF;

Inhibits PT generation, carrier and phase detection;

Inhibits all reports; and

Responds to SEL with END.

Acknowledge (ACKC)

◆ The ACKC command causes the buffer to respond to a good message.

Upon receipt of an ACKC, this unit performs the following functions:

Transmits ACK (1280 cps) for 10 ms; and

Responds to SEL with END at start of tone.

Not-Acknowledge (NAKC)

◆ The NAKC command instructs the buffer to respond to a received message which contained an error. Upon receipt of this command, this unit performs the following functions:

Stores the NAKC

When carrier is removed from the line, it generates and transmits NAK (1920 cps), and responds to SEL with END at start of tone.

Disable (DIS)

◆ The DIS command causes the buffer to remove the Idle current from the line thus rendering it unavailable to the LC. After receipt of this command, the buffer responds to SEL with END. To reinstate this buffer after a DIS, a Halt Device command must be issued prior to the next RC.

Line Control-Command/Response Exchange

◆ The sequence of CCM commands issued for line control purposes and their corresponding buffer responses, depends on the message validation scheme used by the system on the particular line. The following tables show these sequences for CCM and program validation schemes, respectively.

Line Control-Command/Response (Cont'd)

Command/Response Exchange, CCM Validation

	CCM Recognizes	CCM Generates	Buffer Action
Good Message	ETX	ACKC	Transmits ACK (Tone) Responds to SEL with END
Bad Message	Parity error or End and Error	NAKC (not req'd if End and Error)	Inhibits Ready Awaits end of carrier Transmits NAK (Tone) Responds to SEL with End and Error

Command/Response Exchange, Program Validation

	CCM Recognizes	CCM Generates	Program Generates	Buffer Action
Good Message	ETX	TERC	— — — Write Control followed by ACKC or Write Command followed by ACK	Responds with END Sends ACK (Tone) Responds with END
	ETX or End and Error (EER)	TERC (Not req'd if EER)	— — — Write Control followed by NAKC or Write Command followed by NAK (Not req'd if EER)	Responds with END Sends NAK (Tone) Responds with EER

Data Transfer

Initial Conditions

◆ Whenever the buffer receives a SEL from the CCM, it responds with BOP, regardless of command status or line condition. In the absence of a command, this unit remains in the condition in which it is placed upon termination (END) of the previous command. It is then conditioned to receive a new command.

Whenever a signal appears on the Reset lead from the CCM, the buffer is restored to its quiescent condition, the command which was present, if any, is dropped, and Idle current is removed from the line. This unit responds to a subsequent SEL with BOP, only, until another command is received.

Receive

◆ The buffer executes an RC as indicated. When the RT signal from the LC is sensed, and an RC is present, the buffer responds to the LC with PT which conditions the connected IS to initiate transmission.

Carrier is detected by the buffer within 10 ms from the start of PT. Failure to do so causes a Malfunction Report to be sent by this unit to the CCM. Receipt of carrier from the line is considered the beginning of a message. The unmodulated carrier is defined as the logical zero state. After receiving unmodulated carrier for 24 ms the buffer is conditioned to detect phase changes. Interruptions of carrier are sensed and stored as error conditions by this buffer.

When a data bit has been strobed, by means of timing derived from the received signal, the buffer responds to SEL with RDY, and the bit is transferred to the CCM on the Data lead, with the opposite identity (1 for 0 or 0 for 1), as received from the line.

After sending ACK (or NAK), this unit waits for RT to drop (or carrier to reappear), within 1000 ms max. A Malfunction Report is sent to the CCM indicating a line interruption, if the foregoing conditions are not met by the circuit.

The removal of RT by the LC indicates to the buffer that the last message sequence was completed, and a new message sequence can be expected.

Reports

◆ The Report signals to the CCM are encoded by this unit to show Malfunction (MR), Error and End (EER) or END. MRs and EERs terminate the current Receive Command.

Malfunction (MR)

◆ An MR is sent to the CCM whenever the following conditions exist:

1. When RC and RT are present, and carrier is not present for 1000 ms.
2. When 1000 ms have elapsed since the start of ACK, and RT has not been moved from the line.
3. When 1000 ms have elapsed since the start of the second NAK for the same IS (no RT interruptions) and RT has not been removed from the line.

Error and End (EER)

◆ This report is issued by the buffer to indicate that a carrier break was detected after the appearance of the first data bit during the execution of a Read command. The buffer senses and stores the occurrence of a carrier interruption of 3 ms or more, but a report is offered to the CCM only after carrier has been removed from the line for at least one character time. A NAK is automatically generated by the buffer for every EER.

END

◆ This unit reports END, whenever it successfully completes the operations required by each command as previously indicated.

Controls and Indicators

◆ The operator's controls and indicators for the DGS Buffer are located on the CCM Control Panel. They consist of the following:

Data (indicator) - This indicator is lighted whenever the buffer is receiving data signals from an DGS Input Station.

Select (patch panel) - The buffer is easily connected to any CCM Select (SEL) line, and is thereby enabled if power is on. When the buffer is enabled, it responds to each SEL with BOP.

TIME GENERATOR/ BUFFER, MODEL 70/780

◆ The RCA Model 70/780 Time Generator/Buffer (TGB) occupies one scan position of the Communication Controller - Multichannel (CCM), Model 70/668. It is a single integral unit consisting of an electronic clock which generates time-of-day records, and a buffer which transfers the time records bit-serially to the CCM and a Control Panel. The time record consists of four 9-bit, odd-parity, characters. Each character represents one of the digits 0 to 9 in the EBCDIC code. The digits are automatically generated and transferred to the CCM whenever a time change occurs in the least significant digit, provided a Receive Command (RC) is present. The time represented by the digits, in the order transferred, is as follows:

Digit:	1st	2nd	3rd	4th
Hours:	10	10^0	10^{-1}	10^{-2}

The 10^{-2} hours digit represents apparent time as follows:

Minute:	1st	2nd	3rd	4th	5th	6th
Digit:	2	4	5	6	8	0
X 10^{-2}						

The maximum time count is 23.98 hours, with an automatic reset to 00.00 hours as the next increment. Time changes in increments of the apparent 100th of an hour (every 36 seconds) are presented to the CCM by the TGB at 60-second intervals.

An option permits the electronic clock to be synchronized with an external minute-impulse master time system which provides an hourly correction.

OPERATIONAL CHARACTERISTICS

Signals

◆ Control signals and data bits are exchanged between the Time Generator/ Buffer and the CCM in a prescribed sequence:

1. The CCM selects the buffer.
2. The buffer presents its status signals and data level.
3. The CCM issues command signals.
4. The CCM drops Select, allowing the buffer to change its status signals and data level.

Signal and data levels are accepted by the TGB and CCM at Strobe time.

Commands

◆ The command signals from the CCM are decoded by the Time Generator/Buffer into the following commands:

Receive (RC) Terminate (TERC)

Receive

◆ The RC command conditions the Time Generator/Buffer to transfer time-of-day records to the CCM.

Terminate

◆ The TERC command is to terminate an RC. This is the quiescent condition for the Time Generator/Buffer.

Data Transfer

Initial Conditions

◆ Whenever the Time Generator/Buffer receives a SEL from the CCM, it responds with BOP, regardless of command status. In the absence of a command, the buffer remains in the condition in which it was placed upon termination (END) of the previous command, and does not transfer time-of-day records to the CCM. It is then conditioned to receive a new command.

Normal Operation

◆ Through a counter, the clock produces a time pulse derived from the time source which is used to increment the time record stored in a time register. The time record can be set to a desired value through the DIGIT switches. If the time record is set to 00.00, and the clock is started by the START switches, the first time pulse increments the time record to 00.02, the second pulse increments the time record to 00.04, the third to 00.05., ... and the sixth to 00.10. Actual time is converted to the nearest (or apparent) hundredth of an hour.

After the time register has been incremented, and if a Receive command is present, the Time Generator/Buffer responds to a CCM SEL with RDY; and presents the least significant bit of the first digit (10^2 hours) on the Data lead. The remaining bits are presented to the CCM on subsequent SEL's. The bit transfers sequence for each EBCDIC character is: 0, 1, 2, 3, 4, 5, 6, 7, and P. The buffer inhibits RDY after the entire time record has been transferred to the CCM. After this, the buffer does not respond to a CCM SEL with RDY until the clock time register is incremented. RDY is interlocked with the time register incrementation to prevent transfer of partial time records to the CCM.

Operation with Master Time System

◆ When the MASTER-INTERNAL switch is placed in the MASTER position, the clock can be driven from and synchronized with an external minute-impulse master time system. The time register is incremented by an impulse received each minute from the master time system, instead of from its own time pulse. When the time record reaches (optionally) either the 58th (XX.96) or 59th (XX.98) minute, the time register does not increment until an hourly correction signal has been received from the master time system. Upon receipt of a subsequent minute impulse, the time register increments (optionally) to the 59th or 60th minute. If the hourly correction signal arrives early relative to the status of the time register, the register is incremented to the proper time on the subsequent minute impulse. When a master time system is used, the TGB must be synchronized to the exact time of the master time clock or be displaced from it in increments of 60 minutes.

Reports

◆ The Report signals to the CCM are encoded by the Time Generator/Buffer to indicate the following conditions:

Malfunction (MR) END

Malfunction

◆ When a Receive command is present in the Time Generator/Buffer prior to END, the buffer indicates a malfunction condition to the CCM via an MR whenever:

The START-STOP switch is set to the STOP position,

or optionally,

two successive internal time pulses have occurred in the absence of an external minute-impulse.

After an MR, the buffer drops the command which was present and is conditioned to receive a new command.

END

◆ The Time Generator/Buffer reports END after receipt of a TERC from the CCM.

Controls and Indicators

CCM Control Panel

◆ The operator's controls and indicators for the Time Generator/Buffer are located on the CCM Control Panel.

Data (White indicator) - This indicator is lighted whenever a Receive command is present in the buffer.

Select (patch panel) - The Time Generator/Buffer is easily connected to any CCM Select (SEL) line, and is thereby enabled if power is on. When enabled, the buffer responds to an SEL with BOP.

TGB Control Panel

◆ The following controls and indicators are located on the TGB Control Panel:

START-STOP (Switches) - In the START position, this switch locks out the DIGIT and RESET switches. In the STOP position, this switch disables time pulse generation and enables the DIGIT and RESET switches. When returned to the START position, this switch enables the timing function.

RESET (Push-button switch) - This switch is interlocked with the START-STOP switch, and resets all time digits and the time pulse counter to zero.

DIGIT (Four push-button switches) - The DIGIT switches are interlocked with the START-STOP switch, and cause their respective digits to be incremented in the time register. Thus, by using the Readout Displays, the time register can be given an initial setting.

Readout Displays (indicators) - Four sets of four indicators continuously display the binary value of each time digit.

MASTER-INTERNAL (switch) - When in the MASTER position, this switch enables the Time Generator/Buffer to accept minute-impulses and hourly correction from a master time system. When in the INTERNAL position, this switch enables the time register to be incremented by internal time pulses.

Options

◆ The following options can be installed in the field through wiring changes, depending upon the user's requirements. The Time Generator/Buffer is originally conditioned for operation without any of these options.

Master Time System Options

◆ *Cable to Master Time System* - No cable is provided with the TGB to connect to a master time system. Up to 50 feet of suitable wire is used to connect the master time system to the CCM Line Termination Panel. Filters are provided with the TGB, when required.

Hourly Correction - When operating with a master time system, hourly correction is normally performed on the 59th minute. This correction can be changed to the 58th minute.

Program Considerations

◆ After a malfunction (MR) is reported, if a new command is received by the Time Generator/Buffer before the cause of the malfunction is removed, the buffer again issues an MR.

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System Spectra 70 **Date** June 14, 1968 **No.** 1

70/668 Communication Control Multichannel Reference Manual #70-06-668

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The following additions and corrections for the Model 70/668 and Model 70/700 Series Reference Manual (70-06-668) should be noted immediately:

I. The following note should be placed before Table 1-1 page 1-4:

The table indicates the maximum number of lines permitted and should be used as follows:

If 32 lines are desired for example, the number 32 is located in the Total Lines Permitted column. By reading across to the left, the table indicates that 16 lines, each with a speed up to 2400 bits per second can be accommodated in the high speed line group and 16 lines each with a speed up to 600 bits per second can be accommodated in the low speed group. If the lines in the high speed group are not the highest speed possible (2400 bits per second), say they are all 1200 bit per second lines, the number of lines and the maximum speed per line permitted does not change in any way. In other words, a proposed configuration must fall within one of the eight groupings shown in Table 1-1.

II. The following statements should be added to point number 1 "CCM Device Addresses" on page 1-5:

If the line scan capacity of a CCM is not fully utilized, unused device addresses within a 16 number sequence must <u>not</u> be used for other peripheral devices on the multiplexor including other CCMs. Bit 8 of LSW E of each unused device (line) address must be set to 1 so that any commands to that device address are ignored by the CCM.

III. The following description replaces the third paragraph under Construction of Operational Words, General on page 2-3.

Old paragraph: "Parity is checked ... to the decoding logic."

III. (Cont'd)

New Description:

During CCM transmission (processor write CCW), the parity of each character is checked by the CCM before the character is placed into LSW B bits 0-8 and before the character is sent through the decoding (control character recognition) matrix.

During CCM reception (processor read CCW), each character assembled from a communications line retains its line parity sense despite any expansion and is sent through the control character decoding matrix. Parity is not checked for those characters recognized as control characters (those calling up an operational word).

For transmission and reception a control character with a parity error is no longer a control character; it cannot cause the CCM to access an operational word.

IV. The following operational word information replaces and supersedes the information found in Tables 3-5 and 3-6 on pages 3-17, 18, and 19.

Table 3-5 Operational Word 1 (OW-1)

Bit	Function
2, 1, 0 (action control)	These action control bits, set up the conditions for taking the actions of the following Op Word 1 conditional action bits:

(4, 5)	(9, 10, 11, 12)	(13)
Set / Reset In Data Block	Do not send/send indicated coordination message.	Terminate current channel command word (CCW)

and the following Op Word 2 conditional action bits:

2,	3,	4, 5
set next char. is block parity	set status modifier in SDB	set/reset LSW F14

12, 13	14
Special buffer control	Reset LSW B 15

The following are the action control bit settings and their meaning:

000 Do not take action which may be specified by the conditional action bits Op WD 1: 4, 5; 9, 10, 11, 12; 13 Op WD 2: 2, 3; 4, 5; 12, 13; 14

001 Take the actions specified by the conditional action bits.

010 Take the actions if the sequence counter setting is 01.

Table 3-5 Operational Word 1 (OW-1)

Bit		Function
2, 1, 0 (Cont'd)	011	Take actions if the sequence counter setting is 10.
	100	Take actions if the sequence counter setting is 01 and the character in the character store (LSW-F bits 0-8) is identical to the character in the character transfer store (LSW-B bits 0-8) (that is, the previous control character and the present control character appearing on the line are identical.) If the current character is not identical to the previous character, the sequence counter is reset to 00, but after this, the sequence counter will still be modified as specified by bits 7 & 8. For example if bits 8, 7=11, the sequence counter is advanced from 00 to 01.
	101	Take action if the sequence counter setting is 11 and the character in LSW-F bits 0-8 is identical to the character in LSW-B bits 0-8. If the current control character is not identical to the previous control character, the sequence counter is reset to 00, but will then be modified as specified by bits 7 & 8.
	110 111	These settings are not to be used. (unassigned)
3 (not used)	Not used (Set to zero)	
5, 4 (In data Block)	When the conditions of the action control bits are satisfied, bits 5, 4 set or reset bit 13 of LSW-C, the In Data Block Bit. (The In Data Block bit when set (1) during receive operations permits data characters to be sent to the processor, when reset (0) inhibits sending data characters to the processor. The bit also may be a condition for accessing an operational word - See Figure 1-2, page 1-12. Control characters are not affected by In Data Block but are affected by bit 15 of OP WORD 1.	

OW-1

Table 3-5 Operational Word 1 (OW-1)

Bit	Function
5,4 (Cont'd)	Three bit settings only are allowed for bits 5, 4: 00 Do not set or reset in data block bit 13 of LSW-C. 01 Set In data block bit 13 of LSW-C to 1. 10 Reset In data Block bit 13 of LSW-C to 0.
6 (sequence counter control)	Bit 6 controls changes to the sequence counter as follows: 0 When the condition for action specified by bits 2, 1, 0 is satisfied, the sequence counter is reset and any setting of bits 8, 7, is ignored. When the condition for action is not satisfied, the operation specified by bits 8, 7 is performed. (Hardware resetting of the sequence counter may take place before the action of bits 8, 7. See OW-1 bits 2, 1, 0 = 100, 101). 1 Resetting the sequence counter as called for by bits 8, 7 = 00 is prevented, but any other operation called for by bits 8, 7 is permitted.
8, 7 (sequence counter modification)	Bits 8, 7 change the settings of the sequence counter (LSW F bits 15, 16) based on the conditions for action (bits 2, 1, 0) being satisfied and the setting of bit 6. See bit 6 for a complete description of the conditions under which action will be taken on the following bit configurations:

Bits 7,8 (Cont'd) Sequence Counter Modification	00	Reset sequence counter to 00	Subject to action control bits 2,1,0 and bit 6
	01	Set sequence counter to 01.	
	10	Set sequence counter to 10.	
	11	Advance sequence counter. (see table below)	

Current Setting LSWF 16,15	Setting after being advanced 16, 15
00	01
01	10
10	11
11	00

12, 11, 10, 9 (Coordination message)	0000	Do not originate a coordination message (CM) from this op word. (The 0000 setting and all bit settings here do not prevent automatic hardware generation of coordinate messages, also hardware CM information may be contained in the Op Word generated CM's. (See Table 3-7). The following bit settings (those other than 0000) are placed into bits 2^0 - 2^3 of the communications reporting byte (CRB) of a coordination message (CM) generated when the conditions of the action control bits (2,1,0) are satisfied. (Specifying 0001 causes a good message indication (0001) or a bad message indication (0010) to occur in the CRB (communications reporting byte - 1st byte of a CM)). Hardware may also independently generate either of these two settings in the CRB.
	0001	(Good Message - Good Parity) For systems not using block parity, the 0001 bit setting must be used to send a good message CM if desired when the end of message character (or characters) is detected. If a character in the message had bad parity, it will have been replaced by

Table 3-5 Optional Word 1 (OW-1)

Bit		Function
12, 11, 10, 9 (Coordination message) (cont'd)		an $(FF)_{16}$ and bit 16 of LSW B (error recording) will have been set; whenever LSW B 16 is set, if a good message is requested it is changed to a bad message in the CRB. If a good message has not been requested, the hardware generates bad message CMs only. (Upon CM generation, LSW B 16 is reset to zero). For systems using block parity, a good message and bad message CM's are generated automatically by the hardware, the 0001 bit setting in the OP WORD is not necessary and should not be used.
	0010	(Bad Message - Bad Parity) Because this bit configuration may be automatically generated by the hardware, it should not be used to indicate other "bad messages" say those which are terminated by a CAN (cancel) character unless it is unnecessary to distinguish between bad messages with parity errors and other bad messages. If a bad message CM is requested (OP WORD bit setting 0010) and a parity error (character and/or block) occurs, two bad message CMs are sent: one caused by the request (0010), the other caused by the error.
	0011 through 1111	These settings are available to the program as desired, but certain software systems may by convention reserve some of these settings for specific use.
13 (Terminate CCW)	1	When permitted by the action control bits, terminate the existing channel command word (CCW).
	0	No Action
	The following bits are not subject to the action control bits (2, 1, 0); their functions are performed whenever the OP WORD is called up by a control character:	
14 (Exclude Control Character block parity)	1	Exclude the control character which fetched this Op Word from the block count.
	Note:	This bit and bit 0 of OW 2 must not be both equal to 1.
	0	Include the character in the block parity count. (Use 0 setting for non-block parity systems.)
15 (Delete Control Character)	1	Effective only during a Read CCW, inhibit transfer of the control character to the processor. (Control characters, those characters which fetch Op Words, are transferred to the processor regardless of the In/Out of Data Block setting ((LSWC 13)) unless inhibited by this bit.)
	0	Transfer the control character to the processor.

Table 3-5 Operational Word 1 (OW-1)

Bit		Function
16 (Fetch OW-2)	1	Access (staticize) operational word 2 to accomplish additional operations.
	0	Operational Word 2 is not being used.
17 (Hardware Parity)		This parity bit is set or reset to maintain odd parity for this OP WORD by the hardware upon CCM initialization (the memory loading of the Op Word) and is checked by hardware upon each subsequent access of the Op Word. If a parity error occurs (upon any CCM memory access), the CCM becomes inoperable and must be reinitialized to restart operation.

Table 3-6 Operational Word 2 (OW-2)

Bit		Function
0 (block parity)	1	Reset the block parity accumulator (LSW D bits 0-8).
	Note:	OW-2 bit 0 and OW-1 bit 14 must not both be set equal to 1.
	0	No action.
1 (character count)	1	Reset the character counter (LSW D bits 9-16). (Reserved for test routines).
	0	No action.
2 (next char. is block parity)	1	When permitted by action control, set the "next character is block parity" indicator (LSW B bit 13). When transmitting, the CCM will send its accumulated block parity count to the terminal (the remote device). When receiving the CCM will expect the terminal to send block parity and will then compare the next character on the line with the accumulated block parity count.
	0	No action.
3 (skip CCW in chain)	1	When permitted by action control, set the status modifier bit (LSW E 4). The next standard device byte (SDB) sent by the CCM for the line (upon termination of the current CCW) will have its status modifier bit 2^0 set to 1. If the CCW's are command chained, the processor skips the next CCW and executes the one after that.
	0	No action.
5,4 (Set/reset bit LSW F 14)		When permitted by action control, bits 5,4 set or reset LSW F bit 14 which can affect operational word access for a maximum of 16 operational word pairs determined when the CCM is assembled at the factory. (See figure 1-2.)
	00	No action.
	01	Set LSW F bit 14 to 1. subject to action control bits OW-1 2,1,0.
	10	Reset LSW F bit 14 to 0.
	11	Do not use this bit setting!
	Note:	LSW F 14 is not reset upon command initiation.

Table 3-6 Operational Word 2 (OW-2)

Bit		Function	
6,7,8, 9,10,11 (unused)		Not used. (Set to zero)	
13,12 (special buffer control)		These bits are used for special buffer control of special systems such as the Data Gathering System (DGS); bits 13,12 take action only when permitted by action control.	
	00	No action.	Subject to action control bits
	01	If LSW B 16 is zero (no error recorded), send an ACK (acknowledge) command to the buffer.	
	10	Send a DISC (disconnect) command to the buffer. Use this bit setting only with 70/724 and 70/725 buffers!	
	11	Do not use this bit setting!	
14 (Reset LSW B 15 Feature 5623 only)		When Feature 5623 is installed and when permitted by action control, bit 14 may be used to reset LSW B 15 to zero to indicate an unshift status by the control character accessing this Op Word. This function might be used for any shift control system but is particularly useful for Baudot teletype systems in which the unshift on SPACE and LTRS option has been included. A SPACE character can access an Op Word pair which has bit 14 of OW-2 set which will cause an unshift status by resetting LSW B 15 to zero.	
	0	No action.	
	1	When permitted by action control, indicate an unshift status by resetting LSW B 15 to zero.	
16,15 (unused)		Not used.	
17 (parity)		Odd parity for the Op Word is set by hardware upon loading, and is checked upon each access. (See OW-1 bit 17 for details)	

V. Reference numbers have been added for the operational words shown in Table 2-1 to aid in the explanation of the changes.

The action control bits (2,1,0) of Op Word Examples 2, 3 and 4 should be 000 (no action for conditional action bits). The 001 setting is not necessary because conditional action bits are not involved, also 001 takes about 30us longer to process by the CCM.

Two other changes are noted for Op Word 6:

Bit 6 should be 0; there is no reason for it to be 1.
Bit 13 should be 1 because the EOM sequence should call for command termination.

Note: There may be minor variations in the other examples of operational word construction presented in the CCM manual. Any discrepancies will be resolved in favor of this latest operational word description, and will be included in a reissue of the CCM manual to appear shortly.

Table 2-1. OW-1 Construction Example Number 1 (83-B-X)

OP WD NO.*		1	2	3	4	5	6	7
Receive (1)	Transmit (0)	1	1	1	1	1	1	1
In Data Block (1)	Out of Data Block (0)	0	0	0	0	0	1	0
Sequence Counter (LSW 15, 16)		-	00	01	10	11	-	-
OW Bits		Setting for V	Setting for Z (1st)	Setting for C (1st)	Setting for Z (2nd)	Setting for C (2nd)	Setting for N	Setting for S
2, 1, 0 (Action Control)		001	000	000	000	001	101	001
3		0	0	0	0	0	0	0
4		0	0	0	0	1	0	0
5		0	0	0	0	0	1	0
6		0	0	0	0	0	0	0
8,7		00	11	11	11	00	11	00
12-9		0011	0000	0000	0000	0100	0101	0110
13		1	0	0	0	0	1	1
14		0	0	0	0	0	0	0
15		1	1	1	1	1	1	1
16		0	0	0	0	0	0	0
17 (Parity)		-	-	-	-	-	-	-

*Seven individual OW-1s must be constructed for control of this system.